PCI Express® Architecture Configuration Space Test Specification Revision 2.0

August 25, 2008



Revision	Revision History	Date
1.0	Initial release.	4/26/2004
1.1	Updated for 1.1 test updates/additions	12/3/2006
2.0	Updated for PCI Express 2.0	8/25/2008

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1. Introduction

This document primarily covers PCI Express testing of root complexes, switches, bridges, and endpoints for the standard configuration mechanisms, registers, and features in Chapter 7 of the *PCI Express Base Specification, Revision 2.0*. This specification does not describe the full set of PCI Express tests and assertions for these devices.

In particular, devices must also meet the requirements and tests described in the latest versions of the following documents as well as any other tests provided by the PCI-SIG:

PCI Express Architecture PHY Test Specification
Platform BIOS Test Considerations for the PCI Express Architecture
PCI Express Architecture Link Test Specification
PCI Express Architecture Transaction Test Specification

The test assertions provide a complete list of the requirements that are covered by this document. The test descriptions can be referenced to obtain specific details on how the assertions will be tested or for more information when the assertions by themselves are unclear. Some test descriptions include "the test fails if" sections that provide a partial list of some of the specific conditions that would cause the test to fail.

1.1. Coverage

The Configuration Space Test Consideration for the PCI Express Architecture covers items in Chapter 7 of the *PCI Express Specification, Revision 2.0* and configuration items from other specifications that apply to PCI Express devices.

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2. Test Assertions

Note: Test Assertions with Test Descriptions labeled as N/A are currently not planned for testing in the PCI Express test suite. However, the assertions must still be met.

Note: There are published PCI Express 1.1 checklists. The 1.1 assertions listed here the assertions from the checklists documents tested by configuration test descriptions. The checklists were not updated for PCI Express 2.0. New assertions for the 2.0 specifications are tagged with a "2_" prefix to indicate they are not published in separate checklist documents.

Assertion #	Assertion Description	Test #
Subsection Reference: 6.2.2		
2_SYS.2.2#1	Captured Slot Power Limit Value, Captured Slot Power Limit Scale, Max Payload Size, Active State Power Management Control, Read Completion Boundary, Common Clock Configuration, Extended Synch, Enable Clock Power Management, Hardware Autonomous Width Disable, Hardware Autonomous Speed Disable, all registers in Virtual Channel Capability, all registers in Multi-Function Virtual Channel Capability must not reset by a Function Level Reset.	**Many**
Subsection Reference: 7.1 Configuration Topology		
CFG.1.0#4	The upstream port of a PCI Express Switch must be represented as a logical PCI-to-PCI bridge. The secondary bus represents the switch's internal routing logic.	**Test 1.2**
CFG.1.0#5	Switch downstream ports must be represented as PCI-to-PCI bridges from the switch internal bus to a bus representing the downstream PCI Express link.	**Test 1.2**
CFG.1.0#6	A PCI Express multi-function endpoint device must be mapped to configuration space as a single logical device with one or more logical functions. Function 0 must be present.	**Test 1.2**
CFG.1.0#7	Requirements in the configuration space definition for a device apply to single function devices as well as to each function individually of a multi-function device.	**Test 1.27**
CFG.1.0#8	Only PCI-to-PCI bridges representing switch downstream ports may appear on the internal bus of a switch.	**Test 1.2**
Subsection Reference: 7.2.2 PCI Express Enhanced Configuration Mechanism		

Assertion #	Assertion Description	Test #
CFG.2.2#1	Any bits in the Bus Number field that are not mapped from Memory Address bits must be set to zero.	**Test 1.32**
CFG.2.2#2	A minimum of one Memory Address bit (n = 1) must be mapped to the Bus Number field.	**Test 1.18**
Subsection Reference: 7.3.1 Device Number		
CFG.3.1#1	Devices wishing to implement more than 8 functions at their upstream port must implement one or more Type 1 (PCI-to-PCI Bridge) configuration space headers.	**Test 1.2**
CFG.3.1#2	Devices must respond to all Type 0 Configuration Read Requests regardless of the Device Number specified in the Request.	**Test 2.5**
CFG.3.1#4	Devices wishing to implement more than 8 functions at their upstream port must implement an internal Switch structure using Type 1 (PCI-to-PCI Bridge) configuration space headers with the functions logically mapped as devices connected downstream from the Switch.	**Test 1.2**
Subsection Reference: 7.3.3 Configuration Request Routing Rules		
CFG.3.3#5	A type 1 configuration request with a bus number equal to the secondary PCI bus must be transformed to type zero and forwarded to the downstream PCI bus.	**Test 3.8**
CFG.3.3#6	A type 1 configuration request with a bus number in the range of the secondary PCI bus must be forwarded to the secondary bus without modification.	**Test 3.8**
Subsection Reference: 7.4 Configuration Register Types		
CFG.4.0#1	Any read only register fields (RO) may not be changeable by software.	**Test 1.3**
CFG.4.0#2	Any read-write register fields (RW) must settable and clearable by software. NOTE: In the case where a multi-bit RW field has a restricted set of valid values it is not required to be RW when non-valid values are written.	**Test 1.3**
CFG.4.0#3	Read only status – Write 1 to clear (RW1C) fields must be cleared when written with a one. Otherwise they must be read only.	**Test 1.3**
CFG.4.0#4	Sticky bit – read only fields (ROS) must be read only and cannot be reset by a hot reset. If AUX power consumption is being consumed (by either Aux Power or PME Enable) hot, warm and cold resets must not change the existing value of the field.	**Test 1.3**

Assertion #	Assertion Description	Test #
CFG.4.0#5	Sticky bit – read-write fields (RWS) must be settable and clearable by software. They must not be reset with a hot reset. If AUX power is being consumed (by either Aux Power or PME Enable) hot, warm, and cold resets must not reset the fields. In the case where a multi-bit RW field has a restricted set of valid values, it is not required to be RW when non-valid values are written.	**Test 1.3**
CFG.4.0#6	Sticky bit – Read only status – Write 1 to clear - fields (RW1CS) implemented according to the PCI Express specification must be cleared when written with a one. They must not be reset with a hot reset. If AUX power is being consumed (by either Aux Power or PME Enable) hot, warm, and cold resets must not reset the fields that are explicitly called out elsewhere in the checklist.	**Test 1.3**
CFG.4.0#7	Hardware initialized (HwInit) fields implemented according to the PCI Express specification can only be set by hardware or firmware mechanisms. After initialization they are read only but must be reset with Fundamental reset. Note: HwInit fields may also be implemented as read only. Note: Firmware initialization is only allowed for system integrated devices.	**Test 1.3**
CFG.4.0#8	RsvdP - Reserved and Preserved: Reserved for future RW implementations; registers are read-only and must return 0 when read.	**All Register Tests**
CFG.4.0#9	RsvdZ - Reserved and Zero: Reserved for future RW1C implementations; registers are read-only and must return 0 when read.	**All Register Tests**
2_CFG.7.4#10	HwInit registers are not modified by FLR	**Many**
2_CFG.7.4#11	Sticky registers (ROS, RWS, RW1CS are neither initialized not modified by FLR.	**Many**
2_CFG.7.4#12	All registers other than the specific registers mentioned in Section 6.2.2 and Section 7.4 must get reset by FLR.	**Many**
Subsection Reference: 7.5 PCI-Compatible Configuration Registers		
CFG.5.0#1	All register fields that the PCI Express specification indicates must be hardwired to zero must always read zero.	**Test 1.3**
CFG.5.0#2	All fields must default to any default values specified in the PCI Express specification except for Root Complexes and system integrated devices.	**Test 1.3**

Assertion #	Assertion Description	Test #
Subsection Reference: 7.5.1.2 Status Register (Offset 06h)		
CFG.5.2#2	The capabilities list bit must be set to one.	**Test 1.11**
Subsection Reference: 7.5.1.3 Cache Line Size Register (Offset 0Ch)		
CFG.5.3#2	The Cache Line Size register value must be ignored by PCI Express devices.	**Test 1.12**
Subsection Reference: 7.5.1.5 Interrupt Line Register (Offset 3Ch		
CFG.5.4#1	The interrupt line read-write register must be implemented by all PCI Express devices that use an interrupt pin (have a non-zero Interrupt Pin register)	**Test 1.13**
Subsection References: 7.5.2.1 Base Address Registers (Offset 10h – 24h) 7.5.3.1 Base Address Register (Offset 10h/14h)		
CFG.5.7a#1	A BAR that requests address space must request a minimum of 128 bytes.	**Test 1.18**
CFG.5.7a#2	All PCI Express devices except legacy endpoints must support 64-bit addressing for any base address register that requests prefetchable memory resources.	**Test 1.18**
Subsection Reference: 7.5.3 Type 1 Configuration Space Header		
CFG.5.7b#1	A PCI-to-PCI Bridge structure that represents a Root Port or Switch must have a Type 1 Configuration Space Header.	**Test 1.2**
Subsection Reference: 7.5.3.2 Primary Bus Number (Offset 18h)		
CFG.5.7#1	Primary Bus Number must be implemented as read-write for compatibility with legacy software.	**Test 1.32**
Subsection Reference: 7.5.3.4 Prefetchable Memory Base/Limit (Offset 24h)		
CFG.5.8a#1	The Prefetchable Memory Base and Prefetchable Memory Limit registers must indicate that 64-bit addresses are supported.	**Test1.18**
Subsection Reference: 7.6 Power Management Capability Structure		
CFG.6.0#3	Bits 31, 30, and 27 must be set in the PME Support field for structures representing RC and Switch ports to indicate that PME messages will be forwarded.	**Test 1.16**
CFG.6.0#4 EP	If any of the PME support bits are set, the PME Enable bit must be RWS and control PME generation.	**Test 1.16**
CFG.6.0#5 SW, RC	If PMEs can be generated by the component (as opposed to forwarded), the PME Enable field must be RWS and control PME generation.	**Test 1.16**

Assertion #	Assertion Description	Test #
Subsection Reference: 7.8 PCI Express Capability Structure		
CFG.8.0#1	All PCI Express devices must implement the PCI Express capabilities, device capabilities, device status/control, Link capabilities, and Link Status/Control registers.	**Test 1.2**
CFG.8.0#2	All switch downstream ports and root complex ports that implement a slot are required to implement Slot Capabilities and Slot Status/Control registers.	**Test 1.2**
CFG.8.0#3	Root ports must implement root control/status registers.	**Test 1.2**
Subsection Reference: 7.8 PCI Express Capability Structure		
CFG.8.1#1	The Capability ID must be 10h.	**Test 1.3**
Subsection Reference: 7.8.2 PCI Express Capabilities Register (Offset 02h)		
CFG.8.2#1	The Capability Version must be 1h for products implemented to the 1.0a revision of the specification.	**Test 1.3**
CFG.8.2#2	The Device Type/Port Type must be 0000b for a PCI Express Endpoint device.	**Test 1.3**
CFG.8.2#3	The Device Type/Port Type must be 0001b for a Legacy PCI Express Endpoint device.	**Test 1.3**
CFG.8.2#4	The Device Type/Port Type must be 0100b for a root port of a PCI Express Root Complex.	**Test 1.3**
CFG.8.2#5	The Device Type/Port Type must be 0101b for a upstream port of a PCI Express Switch.	**Test 1.3**
CFG.8.2#6	The Device Type/Port Type must be 0110b for a downstream port of a PCI Express Switch.	**Test 1.3**
CFG.8.2#7	The Device Type/Port Type must be 0111b for a PCI Express-to-PCI/PCI-X bridge.	**Test 1.3**
CFG.8.2#8	The Device Type/Port Type must be 1001b for a Root Complex Integrated Endpoint Device.	**Test1.3**
CGF8.2#9	The Device Type/Port Type must be 1001b for a 1010b Root Complex Event Collector.	**Test 1.3**
CFG.8.2#10	A PCI Express endpoint that requires I/O resources for operation once the OS is loaded must indicate itself as a Legacy PCI Express Endpoint device.	**Test 1.3**
CFG.8.2#11	The Slot Implemented field must correctly indicate whether the port is connected to a functional slot. (Must be 0 if the slot is disabled/non functional.)	**Test 3.3**
2_CFG.8.2#12	Capability Version must be hard wired to 2h for Functions compliant to the 2.0 specification.	**Test 1.3**

Assertion #	Assertion Description	Test #
Subsection Reference: 7.8.3		
2_CFG.8.3#1	Function Level Reset Bit applies to Endpoints only. The Device Type must be PCI Express Endpoint Device, Legacy Endpoint Device or Root Complex Integrated Endpoint.	**Test 1.4**
Subsection Reference: 7.8.4 Device Control Register (Offset 08h)		
CFG.8.4#10	The default value of the Max_Payload_Size field must be 000b (128 bytes).	**Test 1.4**
CFG.8.4#21	The Max_Read_Request_Size field must default to 010b (512 bytes). Devices that do not generate requests larger than 128 bytes may hardwire the field to 000b.	**Test 1.4**
Subsection Reference: 7.8.5 Device Status Register (Offset 0Ah)		
CFG.8.5#7	The Transactions Pending must be zero if a device does not have pending transactions.	**Test 1.4**
Subsection Reference: 7.8.6 Device Link Capabilities Register (Offset 0Ch)		
CFG.8.6#1	Maximum (Supported) Link Speed must be 0001b or 0010b.	**Test 1.5**
CFG.8.6#4	The L0s Exit Latency must accurately indicate the length of time the ports takes to transition from L0s to L0 with the current reference clock configuration.	**Test 1.5**
CFG.8.6#6	Each switch link must report a unique port number.	**Test 1.5**
CFG.8.6#7	The upstream port of a switch must report port number zero.	**Test 1.5**
2_CFG.8.6#8	Multi-Function devices must report the same Supported (Maximum) Link Speed value for all Functions.	**Test 1.5**
2_CFG.8.6#9	Multi-Function devices must report the same Maximum Link Width value for all Functions.	**Test 1.5**
2_CFG.8.6#10	Multi-Function devices must report the same ASPM support for all Functions.	**Test 1.5**
2_CFG.8.6#11	Multi-Function devices must report the same L0 Exit Latency for all Functions.	**Test 1.5**
2_CFG.8.6#12	Multi-Function devices must report the same L1 Exit Latency for all Functions.	**Test 1.5**
2_CFG.8.6#13	Multi-Function devices must report the same Port Number for all Functions.	**Test 1.5**
2_CFG.8.6#14	Link Band Width Notification Capability must be Set (1b) for Root Ports and Switch Downstream Ports that support a link speed of 5 GT/s or link width greater than x1.	**Test 1.5**

Assertion #	Assertion Description	Test #
2_CFG.8.6#15	For all devices other than Root Ports and Downstream switch ports, Link Bandwidth Notification Capability must be 0.	**Test 1.5**
Subsection Reference: 7.8.7 Device Link Control Register (Offset 10h)		
CFG.8.7#2	A receiver must be capable of entering L0s even when ASPM control is disabled.	**Test 1.3 + ...**
CFG.8.7#3	Setting the Link Disable bit must disable the link. This is reserved for endpoint devices and upstream ports of a switch.	**Test 3.10**
CFG.8.7#4	Upstream switch and endpoint ports must implement the Link Disable bit as a reserved field and must not be disabled by a write to the field.	**Test 1.5**
CFG.8.7#5	The Retrain Link bit must always return zero when read.	**Test 1.5**
CFG.8.7#6	Setting the Retrain Link bit must initiate link retraining by directing the Physical Layer LTSSM to the Recovery state. The link must enter this state before the completion for the write of the link retraining bit is sent.	**Test 3.8**
CFG.8.7#7	Upstream switch and endpoint ports must implement the Retrain Link bit as a reserved field and must not retrain the link if a 1 is written to the field.	**Test 1.5**
CFG.8.7#12 SW	The RCB field must be hardwired to zero.	**Test 1.5**
Subsection Reference: 7.8.8 Device Link Status Register (Offset 12h)		
CFG.8.8#1	Current Link Speed value must be 0001b for 2.5 GT/s PCI Express Link and 0010b for 5.0 GT/s PCI Express Link.	**Test 1.5**
CFG.8.8#2	The Negotiated Link Width field must correctly indicate the negotiated width of the PCI Express Link.	**Test 2.2** **Test 3.8**
2_CFG.8.8#3	Multi-Function devices must report the same Slot Clock Configuration value for all Functions.	**Test 1.5**
Subsection Reference: 7.8.15		
2_CFG.8.15#1	Completion Timeout Ranges Supported must be 0000b, 0001b, 0010b, 0011b, 0110b, 0111b, 1110b, or 1111b.	**Test 1.40**
Subsection Reference: 7.8.19		
2_CFG.8.18#1	Target Link Speed must be 0001b or 0010b.	**Test 1.41**

Assertion #	Assertion Description	Test #
Subsection Reference: 7.9 PCI Express Extended Capabilities		
CFG.9.0#1	The first DWORD of the capability structure identifies the capability/version and points to the next capability	**Test 1.24**
Subsection Reference: 7.9.1 Extended Capabilities in Configuration Space		
CFG.9.1#1	Extended capabilities in a device configuration space must begin at offset 100h with a PCI Express Enhanced Capability Header.	**Test 1.24**
CFG.9.1#2	Absence of any extended capabilities must be indicated by and Enhanced Capability Header with a Capability ID of 0000h, Capability Version of 0h, and Next Capability Offset of 0h.	**Test 1.24**
Subsection Reference: 7.9.2 Extended Capabilities in the Root Complex		
CFG.9.2#1	Extended capabilities in a Root Complex Register Block always begin at offset 0h with a PCI Express Enhanced Capability Header.	**Test 3.9**
CFG.9.2#2	Absence of any extended capabilities in the Root Complex Register Block must be indicated by an Enhanced Capability Header with a Capability ID of 0xFFFFh and Next Capability Offset of 0h.	**Test 3.9**
Subsection Reference: 7.9.3 Enhanced Capability Register		
CFG.9.3#1	The PCI Express Extended Capability ID field of a PCI Express Enhanced Capability Header must be a valid PCI-SIG defined ID number (or 0xFFFFh or 0x0000h for a terminating header).	**Test 1.7**
CFG.9.3#2	The Capability Version field of a PCI Express Enhanced Capability Header must correctly indicate the version of the capability structure present.	**Test 1.7**
CFG.9.3#3	The Next Capability Offset field must be 000h (termination) or greater than 0FFh.	**Test 1.7**
Subsection Reference: 7.10 Advanced Error Reporting Capability		
CFG.10.0#1	Mask bits corresponding to fields that are not implemented in the Advanced Error Reporting Capability structure must be hard wired to zero.	**Test 1.7**
CFG.10.0#2	Optional error reporting bit fields must consistently be implemented across the Status, Mask, and Severity registers if the mask bit is implemented.	**Test 1.7**

Assertion #	Assertion Description	Test #
Subsection Reference: 7.10.1 Advanced Error Reporting Capability Header (Offset 00h)		
CFG.10.1#1	The PCI Express Extended Capability ID field must be 0001h for an Advanced Error Reporting Capability.	**Test 1.7**
CFG.10.1#2	The Capability Version field must be 1h or 2h per ECN (PCI Express Capability Structure Expansion ECN) for the *PCI Express Base Specification, Revision 1.1*.	**Test 1.7**
Subsection Reference: 7.10.2 Uncorrectable Error Status Register (Offset 04h)		
CFG.10.2#1	The following uncorrectable error fields are required and must be implemented in the Uncorrectable Error Status, Mask, and Severity registers: Data Link Protocol Error, Poisoned TLP, Completion Timeout, Unexpected Completion, Malformed TLP, Unsupported Request Error.	**Test 1.7**
CFG.10.2#5	All the Uncorrectable Error Status fields must default to zero.	**Test 1.7**
Subsection Reference: 7.10.3 Uncorrectable Error Mask Register (Offset 08h)		
CFG.10.3#1	All the Uncorrectable Error Mask fields must default to zero.	**Test 1.7**
CFG.10.3#3	The following uncorrectable error mask fields are optional. If they are implemented the corresponding Uncorrectable Error Severity and Status fields must be implemented: Flow Control Protocol Error, Completer Abort, Receiver Overflow, ECRC Error, Surprise Down Error Mask	**Test 1.7**
Subsection Reference: 7.10.4 Uncorrectable Error Severity Register (Offset 0Ch)		
CFG.10.4#1	The Data Link Protocol Error Severity, Flow Control Protocol Error Severity, Receiver Overflow Error Severity, Surprise Down Error Severity and Malformed TLP Severity fields of the Uncorrectable Error Severity register must default to one.	**Test 1.7**
CFG.10.4#2	The Poisoned TLP Severity, Completion Timeout Error Severity, Completer Abort Error Severity, Unexpected Completion Error Severity, ECRC Error Severity, and Unsupported Request Error Severity fields must default to zero.	**Test 1.7**
Subsection Reference: 7.10.5 Correctable Error Status Register (Offset 10h)		
CFG.10.5#1	The following correctable error fields are required and must be implemented in the Correctable Error Status and Mask registers: Bad TLP Status, Bad DLLP Status, REPLAY_NUM Rollover Status, Replay Timer Timeout Status, Receiver Error Status, Advisory Non-Fatal Error Status.	**Test 1.7**

Assertion #	Assertion Description	Test #
CFG.10.5#4	Correctable Error status fields must only be cleared when software writes a one to the respective bit.	**TBD**
CFG.10.5#5	All the Correctable Error Status fields must default to zero.	**Test 1.7**
Subsection Reference: 7.10.6 Correctable Error Mask Register (Offset 14h)		
CFG.10.6#1	The following Correctable Error Mask fields must default to zero: Receiver Error Mask, Bad TLP Mask, Bad DLLP Mask, REPLAY_NUM Rollover Mask, Replay Timer Timeout Mask	**Test 1.7**
CFG.10.6#2	Advisory Non-Fatal Error Mask – This bit is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.	**Test 1.7**
Subsection Reference: 7.11 Virtual Channel Capability		
CFG.11.0#2	If a multi-function device contains a 2.0 MFVC Capability structure, any or all of its functions are permitted to contain a VC Capability structure. Per-function VC Capability structures are also permitted for devices inside a Switch that contain only Switch Downstream Port functions, or for Root Complex Integrated Devices. Otherwise, only function 0 is permitted to contain a VC Capability structure.	**Test 1.8**
Subsection Reference: 7.11.1 Virtual Channel Enhanced Capability Header		
CFG.11.1#1	A Virtual Channel Capability must use one of two Extended Capability IDs: 0002h or 0009h.	**Test 1.8**
CFG.11.1#2	The Capability Version must be 1h for devices implemented to the *PCI Express Specification, Revision 1.1*.	**Test 1.8**
Subsection Reference: 7.11.2 Port VC Capability Register 1		
CFG.11.2#2	The Low Priority Extended VC Count field must indicate the number of VCs besides VC zero that belong to the lowest priority group if strict priority VC arbitration is being used.	**Test 1.8**
CFG.11.2#3	The Reference Clock field must be hardwired to zero.	**Test 1.8**
CFG.11.2#5	The Port Arbitration Table Entry Size field must accurately indicate the size of the port arbitration field.	**Test 1.8**
CFG.11.2#6	The Port Arbitration Table Entry Size must be zero.	**Test 1.8**
Subsection Reference: 7.11.3 Port VC Capability Register 2		
CFG.11.3#2	The VC Arbitration Table Offset field must be set to zero if no arbitration table is present.	**Test 1.8**
CFG.11.3#3	The VC Arbitration Table Offset field must accurately indicate the offset of a table if one exists.	**Test 1.8**

Assertion #	Assertion Description	Test #
Subsection Reference: 7.11.4 Port VC Control Register		
CFG.11.4#1	Setting the load VC Arbitration Table field must cause hardware to load new settings from the table .	**Test 1.8**
Subsection Reference: 7.11.5 Port VC Control Register		
CFG.11.5#1	Hardware must set the VC Arbitration Table Status field whenever software modifies any entry of the VC Arbitration Table.	**Test 1.8**
CFG.11.5#2	Hardware must clear the VC Arbitration Table Status whenever it finished downloading new values to the VC Arbitration Table.	**Test 1.8**
Subsection Reference: 7.11.6 VC Resource Capability Register		
CFG.11.6#4	The Maximum Time Slots field must accurately indicate the number of slots the resource is capable of supporting when configured for WRR Port Arbitration.	**Test 1.8**
CFG.11.6#5	The Port Arbitration Table Offset field must be set to zero if no arbitration table is present.	**Test 1.8**
CFG.11.6#6	The Port Arbitration Table Offset field must accurately indicate the offset of a table if one exists.	**Test 1.8**
Subsection Reference: 7.11.7 VC Resource Control Register		
CFG.11.7#1	The default value of the TC/VC Map field for the first VC resource must be FFh.	**Test 1.8**
CFG.11.7#2	The default value of all TC/VC Map fields for all resources except the first must be zero.	**Test 1.8**
CFG.11.7#4	Setting the Load Port Arbitration field must cause hardware to load a new port arbitration table if the table is used by the current arbitration scheme.	**Test 1.8**
CFG.11.7#6	The VC ID for the first VC resource must be hardwired to zero.	**Test 1.8**
CFG.11.7#7	Hardware must use the VC ID value for the VC when it is enabled if it is not VC zero.	**TBD**
CFG.11.7#8	The VC Enable field must be hardwired to one for the first VC resource.	**Test 1.8**
CFG.11.7#9	The VC Enable must accurately indicate if the VC is enabled when read. (1 = enabled)	**TBD**
CFG.11.7#10	Writing a one to the VC Enable field must enabled a disabled VC. (Both sides of the link must be updated.)	**TBD**

Assertion #	Assertion Description	Test #
CFG.11.7#11	Writing a zero to the VC Enable field must disable an enabled VC. (Both sides of the link must be updated.)	**TBD**
CFG.11.7#12	Bit 0 of the TC/VC map field is Read only. It must be set to 1 for the default VC0 and set to 0 for all other enabled VCs.	**Test 1.8**
Subsection Reference: 7.11.8 VC Resource Status Register		
CFG.11.8#1	The Port Arbitration Table Status field must be set by hardware whenever an entry in the Port Arbitration table is set.	**Test 1.8**
CFG.11.8#2	Hardware must clear the Port Arbitration Table Status if it successfully downloads a new port arbitration field.	**Test 1.8**
Subsection Reference: 7.11.9 VC Arbitration Table		
CFG.11.9#1	If the default VC resource uses a default VC Arbitration method that uses the VC arbitration table the table must contain all zeros by default.	**Test 1.8**
Subsection Reference: 7.12.1 Device Serial Number Enhanced Capability Header (Offset 00h)		
CFG.12.1#1	The PCI Express Extended Capability ID field for the Device Serial Number Capability is 0003h.	**Test 1.9**
CFG.12.1#2	The Capability Version must be 1h for devices implemented to the *PCI Express Specification, Revision 1.1*.	**Test 1.9**
CFG.12.1#3	The Device Serial Number Capability is optional.	**Test 1.9**
Subsection Reference: 7.12.1 Serial Number Register (Offset 04h)		
CFG.12.2#1	The PCI Express Device Serial Number field must contain a 64 bit unique identifier using EUI-64™.	**Test 1.9**
Subsection Reference: 7.15.1 Power Budgeting Enhanced Capability Header (Offset 00h)		
CFG.13.1#1	The PCI Express Extended Capability ID field for the Power Serial Number Capability is 0004h.	**Test 1.10**
CFG.13.1#2	The Capability Version must be 1h for devices implemented to the *PCI Express Specification, Revision 1.1*.	**Test 1.10**
CFG.13.1#3	The Power Budgeting Enhanced Capability is optional.	**Test 1.10**
Subsection Reference: 7.15.2 Data Select Register (Offset 04h)		
CFG.13.2#1	The Data Select register must be a zero based offset into the Power Budgeting data that controls the DWORD that appears in the Data register.	**Test 1.10**

Assertion #	Assertion Description	Test #
Subsection Reference: 7.15.3 Data Register (Offset 08h)		
CFG.13.3#1	The Data register must contain the DWORD indicated by the Data Select register index or all zeros if the index exceeds the size of the Power Budgeting data.	**Test 1.10**
CFG.13.3#6	Devices that implement the Power Budgeting Capability must provide data values for the D0 Max and D0 Sustained power consumption for every rail they consume power from.	**Test 1.10**
2_CFG.13.3#7	Base Power value is multiplied by data scale except when Data Scale equals 00b and Base Power value exceeds EFh. F3-FFh Base Power values are reserved.	**Test 1.10**
Subsection Reference: 7.16 ACS Extended Capability		
2_CFG.16#1	ACS Extended Capability may only be implemented by a Root Port, a Switch Downstream Port, or a multi-function device function.	**Test 1.42**
2_CFG.16#2	ACS Extended Capability is applicable to Switch Upstream port if it is a part of Multi-function device.	**Test 1.42**
2_CFG.16#3	ACS P2P Completion Redirect is required to be Set for all the functions that support ACS P2P Request Redirect.	**Test 1.42**
2_CFG.16#4	If ACS P2P Egress Control is 0b, the value of the Egress Control Vector Size field is undefined.	**Test 1.42**

3

3. Test Descriptions

This document describes only tests that can be run without special purpose test hardware.

3.1. Configuration Register Common Tests (All Components)

The Chapter 7 common tests cover the registers defined in Chapter 7 of the PCI Express specification. There are more than one state in which many of these tests can be run. Many of the tests are run with the device under test in more than one of these states. Each of the states and procedure used to put the component under test into this state are described here. This information is provided to help with debugging in cases where the component under test is not even reaching the desired starting state for the test The individual tests mention which states they are run on – but do not repeat the setup procedure.

3.1.1. Standard Initialization Procedure – Upstream Ports

Note: Test software prevents the operating system PCI/PCI Express stack from interacting with the device under test once the initialization sequence has started.

D0 – Un-initialized State:

1. Bus is Reset.
2. Software sleeps for 100 milliseconds.
3. The target link speed field is set to the target speed for the test (either 2.5 GT/s or 5.0 GT/s) on the root port of the system slot.

 Note that the packets (TLP/DLLP/Training Sets) from the root port may have any bits set that are defined in the *PCI Express Base Specification, Revision 2.0* but were reserved in previous revisions of the specification.
4. Test software sets the retrain link bit in the Link Control register of the system slot.
5. Device BAR registers are configured to valid regions available in the system.

 Note: Bus Mastering, Interrupts, and PME are not enabled as part of the default configuration procedure.
6. Memory Space and I/O Space Enable are set as appropriate transitioning device to D0 – Initialized State.
7. Autonomous speed and bandwidth changes are disabled for all test cases unless explicitly noted.

D0 - Initialized State:

As part of default test state initialization Active State Power Management is disabled for both upstream and downstream components.

Active State Power Management: Some tests vary the Active State Power Management state of the upstream component under test and downstream port it is connected to. In those tests Active State PM is set at this stage in the initialization process.

Downstream Port: Active Sate Link PM Control field of Link Control register is set as appropriate.

Upstream Port: Active Link PM Control field of Link Control register is set as appropriate.

3.1.2. Standard Register Characteristic Test Routines.

The tests in this specification cover multiple PCI and PCI Express registers and capabilities. A common part of many of these tests is to check register characteristics of each field in the register or capability under test. General procedures for testing register characteristics are given in this section. Individual test descriptions refer to this section.

The tests described below can be performed using accesses of different sizes. The smallest access that can be performed (read/write) is one byte. Two byte and 4 byte accesses can also be performed. If a 3 bit field is being tested, the test could use 1, 2, or 4 byte accesses in performing the test. The specific test descriptions will mention which options are used in testing each individual field.

3.1.2.1 Read Only (RO) Register Field Testing

a. The initial field value is read.

b. The inverse of the value read is written to the field under test. The field under test is inverted – other values are preserved. The write may either succeed or fail as an unsupported request. There is no requirement that the request produce an error response from the device under test.

c. The field value is read. The value must be unchanged from the value read in step a.

d. A binary value of all 1's is written to the field under test.

e. The field value is read. The value must be unchanged from the value read in step a.

Note: RO registers may be implemented as HwInit for Root Complex and Root Complex Embedded Device registers. Test software that will execute on these device types before all system firmware has run on system startup must allow for an RO register to be writable once.

3.1.2.2 Read Write (RW) Register Field Testing

There are two types of RW register field testing. The first type of testing involves writing all valid values to each RW register field and verifying that the value written is read back. These cases are documented in individual test descriptions. The second type of testing involves writing illegal values to RW register fields and monitoring hardware behavior. The following test description describes an invalid value RW register procedure that is performed on all RW register fields documented in the PCI Express specification.

a. The device is placed in the d0-unitialized state. (BARs are not configured).

Note: This test only applies with the device is in the D0 un-initialized state and its BAR registers have not been configured.

b. The initial value is read from the RW field under test.

c. Any illegal value is written to the RW field under test.

Note: The test does not check that the illegal value is latched by the field under test. This is not a requirement.

d. The original value read in step b is written to the device.

e. The Device is configured to the initialized state following the procedure in 3.1.2/3.1.3. The configuration process must still work correctly.

3.1.2.3 Read Write 1 Clear (RW1C) Register Field Testing

a. The initial value is read from the register field under test.

b. The test software writes 1 to the RW1C field under test.

c. The test software reads the value from the register field under test.

The value read must be zero.

d. The software writes a 0 to the RW1C field under test.

e. The software reads the RW1C field under test.

f. The value read must be zero.

3.1.2.4 Read Only Sticky (ROS) Register Field Testing

The tests in Section 3.1.2.1 for a RO register are repeated.

The following additional tests are then performed:

a. The link disable bit on the parent bridge of the device under test (or the bridge under test if it is the root) is set.

b. After 50 milliseconds the link disable bit on the parent bridge of the device under test is cleared.

c. The register under test is read. The value must not have changed.

Note: Special cases where values need to be maintained through more than just hot resets are called out specifically in individual test descriptions later in this specification.

3.1.2.5 Read Write Sticky (RWS) Register Field Testing

The RW test described in Section 3.1.2.2 is performed normally. The following additional testing is performed to verify the sticky nature of the register:

a. The initial value is read from the RW field under test.

b. Any legal value is written to the RW field under test.

c. The RW field is read. The value read must match the value written in step b.

d. The link disable bit on the parent bridge of the device under test (or the bridge under test if it is the root) is set.

e. After 50 milliseconds the link disable bit on the parent bridge of the device under test is cleared.

f. The RW field is read. The value must match the value read in step c.

Note: Special cases where values need to be maintained through more than just hot resets are called out specifically in individual test descriptions later in this specification.

3.1.2.6 Read Write 1 Clear Sticky (RW1CS) Register Field Testing

The following steps are performed in addition to the testing in Section 3.1.2.3:

a. The value in the field under test is read.

b. The link disable bit on the parent bridge of the device under test (or the bridge under test if it is the root) is set.

c. After 50 milliseconds the link disable bit on the parent bridge of the device under test is cleared.

d. The value in the field under test is read. It must match the value read in step a.

3.1.2.7 HwInit Register Field Testing

a. The initial field value is read.

b. The inverse of the value read is written to the field under test. The field under test is inverted – other values are preserved. The write may either succeed or fail as an unsupported request. There is no requirement that the request produce an error response from the device under test.

c. The value of the field is read. The value must be unchanged from the value read in step a. If the value is changed steps a-c are repeated. The value is only allowed to change once.

d. A binary value of all 1's is written to the field under test.

e. The field is read. The value must be unchanged from the value read in step c. If the value has changed the test fails.

3.1.2.8 RsvdP Register Field Testing

RsvdP register fields are tested with the same requirements as Read Only register fields with a specified value of zero.

3.1.2.9 RsvdZ Register Field Testing

RsvdZ registers fields are tested with the same requirements as Read Only register fields with a specified value of zero.

3.1.2.10 Function Level Reset Testing

For a function that supports function level reset (as determined by checking the Function Level Reset Capability bit in the Device Control register) – all register tests that use a reset are repeated using a function level reset instead of the standard link disable/link enable reset sequence. The following registers must not be reset by a functional level reset:

Device Capabilities Register

a. Captured Slot Power Limit Value
b. Captured Slot Power Limit Scale

Device Control Register

a. Max_Payload_Size

Link Control Register

a. Active State Power Management Control
b. Read Completion Boundary
c. Common Clock Configuration
d. Extended Synch
e. Enable Clock Power Management
f. Hardware Autonomous Width Disable

Link Control 2 Register

a. Hardware Autonomous Speed Disable

Virtual Channel Capability

a. All registers

Multi Function Virtual Channel Capability

a. All registers

All other registers are tested normally using the function level reset instead of the normal reset procedure used in the standard initialization and test procedures.

3.1.3. Test 1.2 PCI Express Capability Structure Required Registers

This test is run on all device types. The test verifies that the device under test reports a PCI Express Capability structure that implements the required registers for the device type.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Sections 3.1.1 and 3.1.2. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Sections 3.1.1 or 3.1.2.
2. Examine the Capability ID fields for each of the device Capabilities.
3. If a Capability ID of 0x10h is found attempt to read DWORDs from each of the following offsets:
 a. 00h, 04h, 08h, 0Ch, 10h, 14h, 18h, 1Ch, 20h, 24h, 28h, 2Ch, 30h, 34h, 38h
 b. Test software notes if any read attempts fail.
4. Read the Device/Port Type field of the PCI Express Capabilities register.
5. The Next Capability Pointer must be 00h or greater than or equal to 3Ch for all device types.
6. The test runs with the device under test starting in the D0-Unitialized and D0-Initialized states.
7. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- A Capability ID of 0x10h is not found.
- More than ONE capability ID of 0x10 is found.
- A non-zero next capability pointer is less than 3Ch for any device type.
- A register access in the PCI Express capability below 3Ch fails for any device type.

3.1.4. Test 1.3 PCI Express Capabilities Register

This test is run on all device types. The test verifies that the PCI Express Capabilities register is implemented correctly.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read two bytes located at offset 02h in the PCI Express Capability Structure.
3. Perform each of the following checks on the fields of the two bytes read:
 a. Capability Version – Must be 2h.
 b. Device/Port Type – Must be 0000b, 0001b, 0100b, 0101b, 0110b, 0111b,1000b, 1001b, or 1010b.
4. Check to see if the device implements a Type 01h or 00h PCI Configuration Space Header. Perform the following checks:
 a. Type 00h Device type must be endpoint or legacy endpoint.
 b. Type 01h Device type must be RC Root Port, Upstream Switch Port, Downstream Switch Port, PCI Express-to-PCI/PCI-X Bridge, or PCI/PCI-X-to-PCI Express Bridge.
5. Check the device BAR registers to see whether memory and/or IO space are requested. If IO space is requested and memory space is not requested the device type must be Legacy PCI Express Endpoint device. If IO space is not requested the type must not be Legacy PCI Express Endpoint device.
6. If the Slot Implemented field is one the device type must be a Root Complex Root Port or a Downstream Port of a switch.
7. The following register field characteristic tests are performed as described in Sections 3.1.4.x:
 a. Capability ID RO
 b. Next Capability Pointer RO
 c. Capability Version RO
 d. Device/Port Type RO
 e. Slot Implemented HwInit
 f. Interrupt Message Number RO
 g. RsvdP RO-Zero

8. Perform default value checks for the Express Capabilities register fields as follows:
 a. Capability ID 10
 b. Capability Version 2
 c. RsvP 0
9. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- A PCI Express Capabilities register is not present.
- The Capability Version is not correct.
- The Device/Port Type is not of the defined values in the *PCI Express Base Specification, Revision 1.1*.
- The PCI Configuration Space Header type does not match the Device/Port Type.
- A non-Legacy endpoint device requests I/O space through its BAR registers and does not have any memory space requests.
- The Slot Implemented field is one and the device type is not a Root Complex root port or the downstream port of a switch.
- A register field characteristic test fails.

3.1.5. Test 1.4 Device Capabilities, Control, and Status Registers

This test is run on all device types. The test verifies that the PCI Express Device Capabilities, Device Control, and Device Status registers are implemented correctly.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read four bytes located at offset 04h in the PCI Express Capability Structure.
3. Perform each of the following checks on the fields of the four bytes read:
4. Max_Payload_Size_Supported. Must not be 110b or 111 b (Reserved). The test software writes the value read from Max_Payload_Size_Supported into the Max_Payload_Size register. Software ensures the same value is read from the Max_Payload_Size register. This test is repeated for each Max_Payload_Size value less than the value read from Max_Payload_Size_Supported.
5. The following checks are performed based on the Phantom Functions Supported field:
 a. 01b – device must not be part of a multi-function device using function 4, 5, 6, or 7.
 b. 10b – device must not be part of a multi-function device using function 2, 3, 4, 5, 6, or 7.
 c. 11b – device must not be part of a multi-function device.

6. If the Attention Button Present bit is set the device type must be:
 a. PCI Express Endpoint Device
 b. Legacy PCI Express Endpoint device
 c. Upstream Port of PCI Express Switch
 d. PCI Express-to-PCI/PCI-X bridge
7. If the Attention Indicator Present bit is set the device type must be:
 a. PCI Express Endpoint Device
 b. Legacy PCI Express Endpoint device
 c. Upstream Port of PCI Express Switch
 d. PCI Express-to-PCI/PCI-X bridge
8. If the Power Indicator Present bit is set the device type must be:
 a. PCI Express Endpoint Device
 b. Legacy PCI Express Endpoint device
 c. Upstream Port of PCI Express Switch
 d. PCI Express-to-PCI/PCI-X bridge
9. If the Function Level Reset Capability bit is set the device type must be:
 a. PCI Express Endpoint Device
 b. Legacy PCI Express Endpoint device
10. Read the two bytes at Offset 08h (Device control register).
11. Perform default value checks for the Device Control register fields as follows:
 a. Correctable Error Reporting Enable 0
 b. Non-Fatal Error Reporting Enable 0
 c. Fatal Error Reporting Enable 0
 d. Unsupported Request Reporting Enable 0
 e. Enable Relaxed Ordering 1 or 0 (Based on design)
 f. Max_Payload_Size 000b
 g. Extended Tag Field Enable 0
 h. Phantom Functions Enable 0
 i. Aux Power PM Enable 0
 j. Max Read Request Size 2
 k. Bridge Configuration Retry Enable (RsvdP) 0
 l. Note – Default value rules do not apply to root complexes.
12. Read two bytes at offset 0Ah (Device Status register).
13. Perform default value checks for the Device Status register fields as follows:
 a. Correctable Error Detected 0
 b. Non-Fatal Error Detected 0
 c. Fatal Error Detected 0
 d. Unsupported Request Detected 0
 e. Transactions Pending 0
14. Read four bytes at offset 0Ch (Device Capabilities register).

15. Perform default value checks for the Device Capabilities register fields as follows:
 a. Endpoint LOs Acceptable Latency 0
 b. Endpoint L1s Acceptable Latency 0
 c. Role-Based Error Reporting 1
 d. RsvdP 0

16. These checks apply for all components in the test environment. The following register field characteristic tests are performed as described in Sections 3.1.4.x:

Device Capabilities Register

a. Max_Payload_Size Supported	RO
b. Phantom Functions Supported	RO
c. Extended Tag Field Supported	RO
d. Endpoint L0s Acceptable Latency	RO
e. Endpoint L1 Acceptable Latency	RO
f. Attention Button Present	RO
g. Attention Indicator Present	RO
h. Power Indicator Present	RO
i. Captured Slot Power Limit Value	RO
j. Captured Slot Power Limit Scale	RO
k. RsvdP	RO-Zero
l. Role Based Error Reporting	RO
m. Function Level Reset Capability	RO

Device Control Register

a. Correctable Error Reporting Enable	RW
b. Non-Fatal Error Reporting Enable	RW
c. Fatal Error Reporting Enable	RW
d. Unsupported Request Reporting Enable	RW
e. Enable Relaxed Ordering	RW or RO-Zero.
f. Max_Payload_Size	RW or RO-Zero (only if 128 B is the maximum size supported)
g. Extended Tag Field Enable	RW or RO-Zero
h. Phantom Functions Enable	RW or RO-Zero
i. Auxiliary (AUX) Power PM Enable	RWS or RO-Zero
j. Enable No Snoop	RW or RO-Zero
k. Max_Read_Request_Size	RW or RO-Zero
l. Bridge Configuration Retry Enable	(RsvdP) RW or RO-Zero
m. Rsvdp_2	RO-Zero
n. Initiate Function Level Reset	RO-Zero (all except PCI Express-to-PCI/PCI-X Bridge)

Device Status Register

a. Correctable Error Detected	RW1C
b. Non-Fatal Error Detected	RW1C
c. Fatal Error Detected	RW1C
d. Unsupported Request Detected	RW1C
e. AUX Power Detected	RO
f. Transactions Pending	RO

g. RsvdZ RO-Zero

17. The test has the user verify that an Attention Button, Attention Indicator, and/or Power Indicator are present on the component if any of these bits are set.
18. Perform the following default value checks for the Device Capabilities register.
 a. Captured Slot Power Limit Value 0
 b. Captured Slot Power Limit Scale 0
 c. Role Based Error Reporting 1
19. These checks apply for all components in the test environment if no Set_Slot_Power_Limit messages are sent.
20. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- A PCI Express Device Control, Status, or Capabilities register is not present.
- A supported value written to the Max_Payload_Size control field is not read back.
- A reserved value is read from the Max_Payload_Size_Supported field.
- The device is part of a multi-function device that makes the value in the Phantom Functions Supported field illegal.
- The attention button present, attention indicator present, or power indicator present fields are set for a component not allowed to support these indicators.
- A device control register does not contain one of the default values mentioned above and the device is not a root complex.
- A device status register does not contain one of the default values mentioned above.
- The Transactions Pending bit for the device is not zero.
- The Attention Button, Attention Indicator, or Power Indicator presence bits are set incorrectly.
- The Captured Slot Power fields are not set to zero when no power limit messages have been sent since the last reset.
- A register field characteristic test fails.

3.1.6. Test 1.40 Device Capabilities 2, Control 2, and Status 2 Registers

This test is run on all device types. The test verifies that the PCI Express Device Capabilities2, Device Control2 and Device Status 2 Registers are implemented correctly.

Starting Configuration

This test is run with devices starting in the D0-Uninitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read four bytes located at offset 24h in the PCI Express Capability Structure (Device Capabilities 2).
3. Perform each of the following checks on the fields of the four bytes read:
 a. Completion Timeout Ranges Supported must be 0000b, 0001b, 0010b, 0011b, 0110b, 0111b, 1110b, or 1111b.
4. Read 2 bytes located at Offset 28h (Device Control 2).
5. The following default value rules are checked for the Device Control 2 Register.
 a. Completion Timeout Value 0
 b. Completion Timeout Disable 0
 c. These checks do not apply to a root complex.
6. Read 2 bytes located at Offset 2Ah (Device Status 2).
7. The following register field characteristic tests are performed:

 Device Capabilities 2 Register

 a. Completion Timeout Ranges Supported
 (Switch Ports, Event Collector, PCI/PCI-X-to-PCI Express Bridge) RO-Zero
 b. Completion Timeout Disable Supported
 (Switch Ports, Event Collector, PCI/PCI-X-to-PCI Express Bridge) RO-Zero

 Device Control 2 Register

 a. Completion Timeout Value
 (Switch Ports, Event Collector, PCI/PCI-X-to-PCI Express Bridge) RO-Zero
 b. Completion Timeout Value
 (Root Ports, Endpoints, PCI Express-to-PCI/PCI-X Bridges) RO-Zero or RW
 c. Completion Timeout Disable
 (Switch Ports, Event Collector, PCI/PCI-X to PCI Express Bridge) RO-Zero
 d. Completion Timeout Disable
 (Root Ports, Endpoints, PCI Express-to-PCI/PCI-X Bridges) RO-Zero or RW

 Device Status 2 Register

 a. Entire register. All device types. RO-Zero
8. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

3.1.7. Test 1.5 Link Capabilities, Control, and Status Registers

This test is run on all device types. The test verifies that the PCI Express Link Capabilities, Link Control, and Link Status registers are implemented correctly.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read four bytes located at offset 0Ch (Link Capabilities) in the PCI Express Capability Structure.
3. Perform each of the following checks on the fields of the four bytes read:
 a. Maximum Link Speed must be 0001b or 0010b. (All other encodings are reserved)
 b. Active State Link PM Support
 c. Root Complex – Must be 01b or 11b.
 d. All Other Types – Must be 01b or 11b.
 e. L1 Exit Latency – Must not indicate a shorter time than L0s Exit Latency.
 f. Port Number
 i. Downstream Port of a switch – all ports are checked. All numbers must be unique.
4. For a multi-function device that is an upstream port, the following fields in the Link Capabilities register must be the same in all functions:
 a. Supported Link Speeds
 b. Maximum Link Width
 c. ASPM Support
 d. L0s Exit Latency
 e. L1 Exit Latency
 f. Clock Power Management
 g. Port Number
5. The Link Bandwidth Notification Capability field must be one for root ports and switch downstream ports that have a maximum link speed of 0010b or have a maximum link width greater than x1. For all devices types other than root ports and downstream switch ports the Link Bandwidth Notification Capability field must be 0.
6. Read 2 bytes located at Offset 10h (Link Control).
7. Active State Link PM Control – Must be 00b, 01b, or 11b. Test software writes each of the allowed values to this field (00b, 01b, 11b) and makes sure the same value is read back.

8. The following default value rules are checked for the Link Control register:
 a. Link Disable 0
 b. Common Clock Configuration 0
 c. Extended Synch 0
 d. Enable Clock Power Management 0
 e. RsvdP 0
 f. Hardware Autonomous Width Disable 0
 g. Link Bandwidth Management Interrupt Enable 0
 h. Link Autonomous Bandwidth Interrupt Enable 0

 These checks do not apply to a root complex.

9. Read two bytes from Offset 12h (Link Status).

10. Perform each of the following checks on the fields of the two bytes read:
 a. Current Link Speed – Must be 0001b for 2.5 GT/s test cases. Must be 0010b for 5.0 GT/s test cases.
 b. Negotiated Link Width must be one of the following: 000001b, 000010b, 000100b, 001000b, 010000b, 100000b.
 c. Negotiated Link Width must be equal or less than Maximum Link Width
 d. Training Error – Must be zero.
 e. Link Training – Must be zero.
 f. The Slot Clock Configuration field must have identical values for all functions of a multi-function device.

11. The following register field characteristic checks are performed:

Link Capabilities Register

 a. Maximum Link Speed RO
 b. Maximum Link Width RO
 c. Active State Power Management Support RO
 d. L0s Exit Latency RO
 e. L1 Exit Latency RO
 f. Port Number HwInit
 g. Clock Power Management RO
 h. Surprise Down Error Reporting Capable RO
 i. Data Link Layer Link Active Reporting Capable RO
 j. RsvdP RO-Zero
 k. Link Bandwidth Notification Capability RO

Link Capabilities Register Default Value

 a. Registers are checked for valid Ranges.

Link Control Register

 a. ASPM Control RW
 b. Read Completion Boundary (RC and Switch Downstream) RO-Zero
 c. Link Disable RW
 d. Retrain Link – Downstream Ports RW
 e. Retrain Link – Upstream Ports RO
 f. Common Clock Configuration RW
 g. Extended Synch RW

h. Enable Clock Power Management	RW
i. RsvdP	RO-Zero
j. Link Bandwidth Management Interrupt Enable (Upstream Ports)	RO-Zero
k. Link Autonomous Bandwidth Interrupt Enable (Upstream Ports)	RO-Zero
l. Hardware Autonomous Width Disable	RW or RO-Zero
m. Link Bandwidth Management Interrupt Enable (Downstream Ports)	RW or RO-Zero
n. Link Autonomous Bandwidth Interrupt Enable (Downstream Ports)	RW or RO-Zero

Link Status Register

a. Link Training	RO
b. Link Training (PCI Express-to-PCI/PCI-X Bridge)	RO-Zero
c. Negotiated Link Width	RO
d. Data Link Layer Link Active	RO
e. Undefined	RO
f. Link Speed	RO
g. Slot Clock Configuration	HwInit
h. RsvdZ	RO
l. Downstream Ports (if Corresponding Enable is RW):	
i. Link Bandwidth Management Status	RW1C
ii. Link Autonomous Bandwidth Status	RW1C
m. All other cases:	
i. Link Bandwidth Management Status	RO-Zero
ii. Link Autonomous Bandwidth Status	RO-Zero

12. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- A PCI Express Link Control, Status, or Capabilities register is not present.
- The link training or training error bits for a link under test are not zero.
- The Negotiated Link Width is not equal or less than the reported maximum link width.
- The Negotiated Link With or Maximum Link Width are not one of the spec defined values.
- The Read Completion Boundary field is not ready only for a root complex port.
- Active State Link PM Support is not 11b for device type except a root complex port.
- Active State Link PM Support is not 01b or 11b for a root complex port.
- L0s exit latency is 11b.
- L1 exit latency is reported as shorter than L1 exit latency.
- Active State PM Control does not report a spec defined value.
- Active State PM Control register does not accept all legal values (00b, 01b, 11b).
- A register field characteristic test fails.
- A default value check fails in the Link Control field for a non root complex component.
- A default value check fails in the Link Status register.

3.1.8. Test 1.41 Link Capabilities 2, Control 2, and Status 2 Registers

This test is run on all device types. The test verifies that the PCI Express Link Capabilities 2, Link Control 2, and Link Status 2 registers are implemented correctly.

Starting Configuration

This test is run with devices starting in the D0-Uninitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read four bytes located at offset 2Ch in the PCI Express Capability Structure (Link Capabilities 2).
3. Read 2 bytes located at Offset 30h (Link Control 2).
4. Perform each of the following checks on the fields of the two bytes read:
 a. Target Link Speed must be 0001b or 0010b.

 Note: The Target Link Speed may be 0000b if the device supports 2.5 GT/s only.
5. The following default value rules are checked for the Link Control 2 Register.

a.	Target Link Speed	Highest supported speed.
b.	Enter Compliance	0
c.	Hardware Autonomous Speed Disable	0
d.	Transmit Margin	0
e.	Enter Modified Compliance	0
f.	Compliance SOS	0
g.	Compliance De-emphasis	0

 These checks do not apply to a root complex.

 Note: The Target Link Speed may be 0000b if the device supports 2.5 GT/s only.
6. Read 2 bytes located at Offset 32h (Link Status 2)
7. Perform each of the following checks on the fields of the two bytes read:
 a. Current De-emphasis Level must reflect the expected level when operating at 5.0 GT/s. The expected level is determined by the system specific settings for the system used to perform the test.

8. The following register field characteristic tests are performed:

Link Capabilities 2 Register

a. Entire register. All device types. RO-Zero

Link Control 2 Register

a. Target Link Speed RWS (RO-Zero if device supports only2.5 GT/s)
b. Enter Compliance RWS (RO-Zero if device supports only 2.5 GT/s)
c. Hardware Autonomous Speed Disable RWS or RO-Zero
d. Selectable De-emphasis (Endpoints, PCI Express-to-PCI/PCI-X Bridges, Upstream Ports of Switches) RO-Zero
e. Selectable De-emphasis (Upstream components) RO
f. Transmit Margin RWS (May be RO-Zero if component does not support 5.0 GT/s.)
g. Enter Modified Compliance RWS (May be RO-Zero if component does not support 5.0 GT/s.)
h. Compliance SOS RWS (May be RO-Zero if component does not support 5.0 GT/s.)
i. Compliance De-emphasis RWS (May be RO-Zero if component does not support 5.0 GT/s.)

Link Status 2 Register

a. Current De-emphasis Level RO

9. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

3.1.9. Test 1.6 MSI Capability Structure

This test is run on all device types. The test verifies that the PCI Express component reports an MSI capability structure as required by the *PCI Express Base Specification, Revision 1.0* if the device support interrupts. Alternately, the device may report an MSI-X capability structure to cover this requirement.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Two bytes are read from Offset 03Ch in configuration space for the device under test. (Interrupt Line register and Interrupt Pin register)
3. If the Interrupt Pin register is non-zero, the device must support MSI interrupts.
4. Examine the Capability ID fields for each of the device Capabilities.

5. If the Capability ID of 05h is found the following checks are performed on the MSI capability structure
 a. Two bytes are read from offset 02h in the MSI capability structure. (MSI Control register)
 b. If the 64-bit Address Capable field of the Message Control register is set DWORD R/W registers must be implemented at offset 4 and offset 8. Otherwise only a 32 bit address register at Offset 4h must be implemented.
 c. The MSI Enable field must be zero (after reset).
 Note: This requirement does not apply to a root complex.
6. The Multiple Message Capable field most not read 110b or 111b (Reserved).
7. Test software writes each supported value from the Multiple Message Capable into the Multiple Message Enable field. (If Multiple Message Capable reports 001b for two messages, then 001b and 000b are written to the multiple message enable field.)
8. After writing each value test software ensures the same value is read back from the multiple message enable field.
9. The Reserved bits (9:15) must be zero.
10. Test software ensures there is a two byte RW register implemented at offset 8h (32 bit) or offset 0Ch (64 bit) for the Message Data register.
11. The following register field characteristic checks are performed:

Capability ID RO

Next Cap Pointer RO

Message Control Register

a. Multiple Message Capable RO
b. Multiple Message Enable RW
c. 64 Bit Address Capable RO
d. Per-vector masking capable RO
e. Reserved RO-Zero

Message Address Register

a. Reserved (Bits 0:1) RO
b. Message Address RW
c. Message Upper Address register (Only if 64 Bit Address Capable Set)
d. Message Upper Address RW
e. Message Data register
f. Message Data RW

12. The test is repeated with the device is D0-Unitialized and D0-Iniitialized states.
13. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The Interrupt Pin register has a non-zero value and no MSI or MSI-X capability register is present.
- More than one MSI capability register is present.
- The 64 bit Address Capable register field is set but only one DWORD address register is implemented.
- The Multiple Message Capable field reports a reserved value.
- Any of the allowed Multiple Message settings cannot be written to and read back from the Multiple Message Enable field.
- A 2 byte RW Message Data register is not implemented at the proper offset.
- The MSI Enable field is not zero by default (except for a root complex).
- A register field characteristic test fails.

3.1.10. Test 1.7 Advanced Error Reporting

This test is run on all device types. The test verifies that if the PCI Express component reports a PCI Express Advanced Error Reporting Capability structure it is implemented as required by the *PCI Express Base Specification, Revision 1.0*.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Examine the Capability ID fields for each of the device Capabilities.
3. If the Capability ID of 0001h is found the following checks are performed on the Advanced Error Reporting capability structure.
4. DWORDs are read from offsets 00h to 34h to obtain the default values for each of the capability fields. Root Complex ports must implement all fields.
5. The Capability Version field must be 1h.
6. The default values of each of the defined bits in the Uncorrectable Error Status register must be zero.
 Note: This rule does not apply to bits corresponding to mask bits that are not implemented.
 a. This requirement applies to all components except root complexes.
7. Each defined bit in the Uncorrectable Error Mask register must read zero by default. Test software writes a one to each of these bits and verifies that a one is read back. Software notes each bit that cannot be set. (Unsupported uncorrectable error bits.) The test fails if a required bit cannot be set.
8. Software clears all bits.

9. Software checks the default values of each bit in the Uncorrectable Error Severity register defined bits. Software then writes the opposite value to each bit.
 Note: This rule does not apply to bits corresponding to mask bits that are not implemented.

 The default value requirement applies to all components except root complexes.
10. Software resets all bits to the default values.
11. Software checks that all values for defined bits in the Correctable Error Status register are zero.
 Note: This rule does not apply to bits corresponding to mask bits that are n0t implemented.
 The default value requirement applies to all components except root complexes.
12. Software checks that the Correctable Error Mask registers all read zero by default. Software verifies that all bits (with the possible exception of the Receiver Error Mask bit) can be set.
13. The Advanced Error Capabilities and Control register is examined. The ECRC Generation Enable and ERC Check Enable fields must default to zero. If either of the ECRC Check Capable or ECRC Generation capable bits are set, software checks to ensure that the corresponding enable bits are RW and can be set and cleared.

 The default value requirement applies to all components except root complexes.
14. Root Complex Only: Software checks that the Root Error Status registers are zero.
15. The test is repeated with the device is D0-unitialized and D0-iniitialized states.
16. The following register field characteristic tests are performed:

Advanced Error Reporting Enhanced Capability Header (Offset 00h)

a.	PCI Express Extended Capability ID	RO
b.	Capability Version	RO
c.	Next Capability Offset	RO

Uncorrectable Error Status Register (Offset 04h)

a.	Data Link Protocol Error Status	RW1CS
b.	Poisoned TLP Status	RW1CS
c.	Flow Control Protocol Error Status	RW1CS
d.	Completion Timeout Status	RW1CS
e.	Completer Abort Status	RW1CS
f.	Unexpected Completion Status	RW1CS
g.	Receiver Overflow Status	RW1CS
h.	Malformed TLP Status	RW1CS
i.	ECRC Error Status	RW1CS
j.	Unsupported Request Error Status	RW1CS
k.	Surprise Down Error Status	RW1CS
l.	ACS Violation Status	RW1CS
m.	RsvdZ	RO-Zero

Note: These tests do not apply if the corresponding mask is not implemented.

Uncorrectable Error Status Register Default Value (Offset 04h)

a. Data Link Protocol Error Status	0
b. Poisoned TLP Status	0
c. Flow Control Protocol Error Status	0
d. Completion Timeout Status	0
d. Completer Abort Status	0
e. Unexpected Completion Status	0
f. Receiver Overflow Status	0
g. Malformed TLP Status	0
h. ECRC Error Status	0
i. Unsupported Request Error Status	0
j. Surprise Down Error Status	0
k. ACS Violation Status	0
l. RsvdZ	RO-Zero

Note: These tests do not apply if the corresponding mask is not implemented.

Uncorrectable Error Mask Register (Offset 08h)

a. Data Link Protocol Mask	RWS
b. Poisoned TLP Mask	RWS
c. Flow Control Protocol Error Mask	RWS or RO-Zero
d. Completion Timeout Mask	RWS
e. Completer Abort Mask	RWS or RO-Zero
f. Unexpected Completion Mask	RWS
g. Receiver Overflow Mask	RWS or RO-Zero
h. Malformed TLP Mask	RWS
i. ECRC Error Mask	RWS or RO-Zero
j. Unsupported Request Error Mask	RWS
k. Surprise Down Error Mask	RWS
l. ACS Violation Mask	RWS or RO-Zero
m. RsvdP	RO-Zero

Uncorrectable Error Mask Register Default Value (Offset 08h)

a. Data Link Protocol Mask	0
b. Poisoned TLP Mask	0
c. Flow Control Protocol Error Mask	0
d. Completion Timeout Mask	0
e. Completer Abort Mask	0
f. Unexpected Completion Mask	0
g. Receiver Overflow Mask	0
h. Malformed TLP Mask	0
i. ECRC Error Mask	0
j. Unsupported Request Error Mask	0
k. Surprise Down Error Mask	0
l. ACS Violation Mask	0
m. RsvdP	0

Uncorrectable Error Severity Register (Offset 0Ch)

a.	Data Link Protocol Error Severity	RWS
b.	Poisoned TLP Severity	RWS
c.	Flow Control Protocol Error Severity	RWS
d.	Completion Timeout Severity	RWS
e.	Completer Abort Error Severity	RWS
f.	Unexpected Completion Severity	RWS
g.	Receiver Overflow Severity	RWS
h.	Malformed TLP Severity	RWS
i.	ECRC Error Severity	RWS
j.	Unsupported Request Error Severity	RWS
k.	Surprise Down Error Severity	RWS
l.	ACS Violation Severity	RWS
m.	RsvdP	RO-Zero

Note: These tests do not apply if the corresponding mask is not implemented.

Uncorrectable Error Severity Register Default Value (Offset 0Ch)

a.	Data Link Protocol Error Severity	1
b.	Poisoned TLP Severity	0
c.	Flow Control Protocol Error Severity	1
d.	Completion Timeout Severity	0
e.	Completer Abort Error Severity	0
f.	Unexpected Completion Severity	0
g.	Receiver Overflow Severity	1
h.	Malformed TLP Severity	1
i.	ECRC Error Severity	0
j.	Unsupported Request Error Severity	0
k.	Surprise Down Error Severity	1
l.	ACS Violation Severity	0
m.	RsvdP	0

Note: These tests do not apply if the corresponding mask is not implemented.

Correctable Error Status Register (Offset 10h)

a.	Receiver Error Status	RW1CS
b.	Bad TLP Status	RW1CS
c.	Bad DLLP Status	RW1CS
d.	REPLAY_NUM Rollover Status	RW1CS
e.	Replay Timer Timeout Status	RW1CS
f.	Advisory Non-Fatal Error Status	RW1CS
g.	RsvdZ	RO-Zero

Note: These tests do not apply if the corresponding mask is not implemented.

Correctable Error Status Register Default Value (Offset 10h)

a.	Receiver Error Status	0
b.	Bad TLP Status	0
c.	Bad DLLP Status	0
d.	REPLAY_NUM Rollover Status	0
e.	Replay Timer Timeout Status	0
f.	Advisory Non-Fatal Error Status	0

g. RsvdZ	0

Note: These tests do not apply if the corresponding mask is not implemented.

Correctable Error Mask Register (Offset 14h)

a. Receiver Error Mask	RWS or RO-Zero
b. Bad TLP Mask	RWS
c. Bad DLLP Mask	RWS
d. REPLAY_NUM Rollover Mask	RWS
e. Replay Timer Timeout Mask	RWS
f. Advisory Non-Fatal Error Mask	RWS
g. RsvdP	RO-Zero

Correctable Error Mask Register Default Value (Offset 14h)

a. Receiver Error Mask	0
b. Bad TLP Mask	0
c. Bad DLLP Mask	0
d. REPLAY_NUM Rollover Mask	0
e. Replay Timer Timeout Mask	0
f. Advisory Non-Fatal Error Mask	1
g. RsvdP	0

Advanced Error Capabilities and Control Register (Offset 18h)

a. First Error Pointer	ROS
b. ECRC Generation Capable	RO
c. ECRC Generation Enable	RWS only if ECRC Generation Capable otherwise RO
d. ECRC Check Capable	RO
e. ECRC Check Enable	RWS only if ECRC Check Capable; otherwise RO
f. RsvdP	RO-Zero

Advanced Error Capabilities and Control Register Default Value (Offset 18h)

a. ECRC Generation Enable	0
b. ECRC Check Enable	0
c. RsvdP	0

Header Log Register (Offset 1Ch)

a. Header Log register (1st DW)	ROS
b. Header Log register (2nd DW)	ROS
c. Header Log register (3rd DW)	ROS
d. Header Log register (4th DW)	ROS
e. Header of TLP associated with error	ROS

Header Log Register (Offset 1Ch)

a. Header of TLP associated with error	0

Root Error Command Register (Offset 2Ch)

a. Correctable Error Reporting Enable	RW
b. Non-Fatal Error Reporting Enable	RW
c. Fatal Error Reporting Enable	RW
d. RsvdP	RO-Zero

Root Error Command Register Default Value (Offset 2Ch)

a.	Correctable Error Reporting Enable	0
b.	Non-Fatal Error Reporting Enable	0
c.	Fatal Error Reporting Enable	0
d.	RsvdP	0

Root Error Status Register (Offset 30h)

a.	ERR_COR Received	RW1CS
b.	Multiple ERR_COR Received	RW1CS
c.	ERR_FATAL/NON_FATAL Received	RW1CS
d.	Multiple ERR_FATAL/NONFATAL Received	RW1CS
e.	First Uncorrectable Fatal	RW1CS
f.	Non-Fatal Error Messages Received	RW1CS
g.	Fatal Error Messages Received	RW1CS
h.	Advanced Error Interrupt Message Number	RO

Root Error Status Register Default Value (Offset 30h)

a.	ERR_COR Received	0
b.	Multiple ERR_COR Received	0
c.	ERR_FATAL/NON_FATAL Received	0
d.	Multiple ERR_FATAL/NONFATAL Received	0
e.	First Uncorrectable Fatal	0
f.	Non-Fatal Error Messages Received	0
g.	Fatal Error Messages Received	0

Error Source Identification Register (Offset 34h)

a.	ERR_COR Source Identification	ROS
b.	ERR_FATAL/NONFATAL Source Identification	ROS

Error Source Identification Register (Offset 34h)

a.	ERR_COR Source Identification	0
b.	ERR_FATAL/NONFATAL Source Identification	0

Secondary Uncorrectable Error Status Register (Offset 2Ch)

a.	Master-Abort on Split Completion Status	RW1CS
b.	Target-Abort on Split Completion Status (Optional)	RW1CS
c.	Received Target-Abort Status (Optional)	RW1CS
d.	Received Master-Abort Status	RW1CS
e.	Unexpected Split Completion Error Status	RW1CS
f.	Uncorrectable Split Completion Message Data Error Status	RW1CS
g.	Uncorrectable Data Error Status	RW1CS
h.	Uncorrectable Attribute Error Status	RW1CS
i.	Uncorrectable Address Error Status	RW1CS
j.	Delayed Transaction Discard Timer Expired Status	RW1CS
k.	PERR# Assertion Detected	RW1CS
l.	SERR# Assertion Detected	RW1CS
m.	Internal Bridge Error Status	RW1CS
n.	RsvdZ	RO-Zero

Secondary Uncorrectable Error Status Register Default Value (Offset 2Ch)

a.	Master-Abort on Split Completion Status	0
b.	Target-Abort on Split Completion Status (Optional)	0
c.	Received Target-Abort Status (Optional)	0
d.	Received Master-Abort Status	0
e.	Unexpected Split Completion Error Status	0
f.	Uncorrectable Split Completion Message Data Error Status	0
g.	Uncorrectable Data Error Status	0
h.	Uncorrectable Attribute Error Status	0
i.	Uncorrectable Address Error Status	0
j.	Delayed Transaction Discard Timer Expired Status	0
k.	PERR# Assertion Detected	0
l.	SERR# Assertion Detected	0
m.	Internal Bridge Error Status	0
n.	RsvdZ	0

Secondary Uncorrectable Error Mask Register (Offset 30h)

a.	Master-Abort on Split Completion Mask	RWS
b.	Target-Abort on Split Completion Mask (Optional)	RWS
c.	Received Target-Abort Mask (Optional)	RWS
d.	Received Master-Abort Mask	RWS
e.	Unexpected Split Completion Error Mask	RWS
f.	Uncorrectable Split Completion Message Data Error Mask	RWS
g.	Uncorrectable Data Error Mask	RWS
h.	Uncorrectable Attribute Error Mask	RWS
i.	Uncorrectable Address Error Mask	RWS
j.	Delayed Transaction Discard Timer Expired Mask	RWS
k.	PERR# Assertion Detected	RWS
l.	SERR# Assertion Detected	RWS
m.	Internal Bridge Error Mask	RWS
n.	RsvdZ	RO-Zero

Secondary Uncorrectable Error Mask Register Default Value (Offset 30h)

a.	Master-Abort on Split Completion Mask	0
b.	Target-Abort on Split Completion Mask (Optional)	0
c.	Received Target-Abort Mask (Optional)	0
d.	Received Master-Abort Mask	1
e.	Unexpected Split Completion Error Mask	1
f.	Uncorrectable Split Completion Message Data Error Mask	0
g.	Uncorrectable Data Error Mask	1
h.	Uncorrectable Attribute Error Mask	1
i.	Uncorrectable Address Error Mask	1
j.	Delayed Transaction Discard Timer Expired Mask	1
k.	PERR# Assertion Detected	0
l.	SERR# Assertion Detected	1
m.	Internal Bridge Error Mask	0
n.	RsvdZ	0

Secondary Uncorrectable Error Severity Register (Offset 34h)

a.	Target-Abort on Split Completion Severity (Optional)	RWS
b.	Master-Abort on Split Completion Severity	RWS
c.	Received Target-Abort Severity (Optional)	RWS
d.	Received Master-Abort Severity	RWS
e.	RsvdP	RO-Zero
f.	Unexpected Split Completion Error Severity	RWS
g.	Uncorrectable Split Completion Message Data Error Severity	RWS
h.	Uncorrectable Data Error Severity	RWS
i.	Uncorrectable Attribute Error Severity	RWS
j.	Uncorrectable Address Error Severity	RWS
k.	Delayed Transaction Discard Timer Expired Severity	RWS
l.	PERR# Assertion Detected Severity	RWS
m.	SERR# Assertion Detected Severity	RWS
n.	Internal Bridge Error Severity	RWS

Secondary Uncorrectable Error Severity Register Default Value (Offset 34h)

a.	Target-Abort on Split Completion Severity (Optional)	0
b.	Master-Abort on Split Completion Severity	0
c.	Received Target-Abort Severity (Optional)	0
d.	Received Master-Abort Severity	0
e.	RsvdP	0
f.	Unexpected Split Completion Error Severity	0
g.	Uncorrectable Split Completion Message Data Error Severity	1
h.	Uncorrectable Data Error Severity	0
i.	Uncorrectable Attribute Error Severity	1
j.	Uncorrectable Address Error Severity	1
k.	Delayed Transaction Discard Timer Expired Severity	0
l.	PERR# Assertion Detected Severity	0
m.	SERR# Assertion Detected Severity	1
n.	Internal Bridge Error Severity	0

Secondary Error Capabilities and Control Register (Offset 38h)

a.	Secondary Uncorrectable First Error Pointer	ROS
b.	RsvdP	RO-Zero

Secondary Error Capabilities and Control Register Default Value (Offset 38h)

a.	Secondary Uncorrectable First Error Pointer	0
b.	RsvdP	0

Secondary Header Log Register (Offset 3Ch)

a.	Transaction Attribute	ROS
b.	Transaction Command Lower	ROS
c.	Transaction Command Upper	ROS
d.	Transaction Address	ROS
e.	RsvdZ	RO-Zero

Secondary Header Log Register Default Value (Offset 3Ch)

a. Transaction Attribute 0
b. Transaction Command Lower 0
c. Transaction Command Upper 0
d. Transaction Address 0
e. RsvdZ 0

17. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- More than one Advanced Error Reporting capability structures are present.
- A root complex port does not implement the Root Error Command, Root Error Status, or Error Source Identification registers.
- The capability version does not report 01h or 2h (per ECN - PCI Express Capability Structure Expansion ECN).
- The Uncorrectable Error Status register reports an error. (After standard legal configuration performed by the test).
- A required bit in the Uncorrectable Error Mask register cannot be set.
- Any of the defined fields (bits) in the Correctable Error status register report an error. (After standard legal configuration performed by the test).
- Any required Mask register fields cannot be set and cleared in the Correctable Error Mask.
- ECRC Check Capable or ECRC Generation Capable are set and the corresponding enable field cannot be set and cleared.
- The Root Error Status register reports an error.
- A register field characteristic test fails.
- A default value check fails for any component except a root complex.

3.1.11. Test 1.8 Virtual Channel Capability

This test is run on all device types. The test verifies that if PCI Express component reports a PCI Express Virtual Channel Capability structure it is implemented as required by the *PCI Express Base Specification, Revision 2.0*.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Examine the Capability ID fields for each of the device Capabilities.
3. If the Capability ID of 0002h is found the following checks are performed on the Virtual Channel Capability Structure Error Reporting capability structure

4. Software reads the DWORD at offset 04h (Port VC Capability Register 1) and performs the following checks:
 a. Checks that the Low Priority Extended VC Count is less than or equal to the Extended VC count.
 b. The Reference Clock field must be zero.
5. Software reads the DWORD from offset 08h (Power VC Capability Register 2) and performs the following checks:
 a. No reserved bits (4-7) in the VC Arbitration Capability field may be set.
 b. The VC Arbitration Capability field must not be zero if the Low Priority Extended VC Count is non-zero.
 c. The VC Arbitration table offset must not be zero if any bit besides bit zero of the VC Arbitration Capability field is set.
6. Software reads the DWORD from offset 0Ch (Port VC Control and Port VC Status) and performs the following checks:
 a. VC Arbitration Table Status reads zero by default.
7. If the default VC Arbitration Select value is a WRR based arbitration method software reads the default values in the VC Arbitration table. These values must all be zero.
8. Software writes each of the supported values indicated by the VC Arbitration Capability field to the VC Arbitration Select field and verifies the value is read back.
9. For each supported WRR arbitration field mechanism software tests loading the table by writing a table of all zeroes of the appropriate size to the indicated VC Arbitration table offset. Software then checks that the VC Arbitration Table Status bit has been set. Software then writes the Load VC Arbitration Table field and verifies that the VC Arbitration Table Status bit is cleared by hardware.
10. Step 9 is repeated using all VC entries for the highest supported VC instead of zero.
11. Software verifies that VC Resource Control, Status, and Capability registers are present for each VC supported by the component (as indicated by Extended VC Count field).
12. For each Set of VC Control, Status, and Resource Capability registers software performs the following checks:
 a. Port Arbitration Capability: Switch port or RCRB – Must not have bit 6 or 7 set (reserved).
 b. Port Arbitration Table Offset. Switch or RCRB – Must be nonzero if Port Arbitration Capability indicates any WRR based methods. Other component – must be zero.
 c. TC/VC Map: Must be FFh for the first VC Resource by default. All other VCs – must be zero by default. Software writes each valid TC combination to the field and ensures that the same value can be read back.
 d. This default value restriction does not apply to an RCRB.
 e. Load Port Arbitration Table: Must be zero.
 f. Port Arbitration Select: Software writes each supported value from the Port Arbitration Capability field and ensure that the same value is read back.
 g. VC-ID: Software ensures that the value is hard-wired to zero for the first VC Resource.
 h. VC Enable: Software checks that this bit is hardwired to one for the first VS resource.
 i. Port Arbitration Table Status: Must be zero.

13. For each supported WRR based Port Arbitration scheme software writes a table with all values of the minimum port number. After the first write to the table, software verifies that the Port Arbitration Table Status field is set. Software sets the Load Port Arbitration field. Software verifies that the Port Arbitration Table Status bit is clear.
14. Step 13 is repeated with a valid arbitration table containing all ports on the switch.
15. The following register field characteristic tests are performed:

Virtual Channel Enhanced Capability Header

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Port VC Capability Register 1

a. Extended VC Count	RO
b. Low Priority Extended VC Count	RO
c. Reference Clock	RO
d. Port Arbitration Table Entry Size	RO

Port VC Capability Register 2

a. VC Arbitration Capability	RO
b. VC Arbitration Table Offset	RO

Port VC Control Register

a. VC Arbitration Select	RW if more than one option in Arbitration Capability

Port VC Status Register

a. VC Arbitration Table Status	RO

VC Resource Capability Register (n)

a. Port Arbitration Capability	RO
b. Advanced Packet Switching	RO
c. Reject Snoop Transactions	HwInit
d. Maximum Time Slots	HwInit
e. Port Arbitration Table Offset	RO

VC Resource Control Register (n)

a. TC/VC Map	RW (except bit zero – RO)
b. Port Arbitration Select	RW if more than one option indicated in Port Arbitration Capability
c. VC_ID	RO for VC0
d. VC_ID	RW for all non VC0
e. VC Enable – VC0	RO

VC Resource Status Register (n)

a. Port Arbitration Table Status	RO
b. VC Negotiation Pending	RO

16. The test is repeated with the component in the D0-Unitialized and D0-Initialized states.

17. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- More than one Virtual Channel capability structures are present.
- A switch has Virtual Channel Capability structures for some ports but not others.
- The Low Priority Extended VC Count is greater than the Extended VC count. (Port VC Capability Register 1)
- The reference clock field is not zero. (Port VC Capability Register 1)
- The VC Arbitration Capability field contains a reserved value and the Low Priority Extended VC count field is non-zero.
- The VC Arbitration Table Offset is zero when WRR based VC Arbitration Capabilities are supported.
- VC Arbitration Table Status reads non-zero by default.
- The default VC Arbitration Select value is an WRR based arbitration method and the default VC Arbitration table values are not all zero.
- VC Resource Control, Status, and Capability registers are not present for each VC supported by the component (as indicated by Extended VC Count field).
- A valid Port Arbitration or VC Arbitration table cannot be written.
- Any of the described VC Resource, Control, Status register value checks are not met.
- Any register field characteristic tests fail.

3.1.12. Test 1.9 Device Serial Number Capability

This test is run on all device types. The test verifies that if PCI Express component reports a PCI Express Device Serial Number Capability structure it is implemented as required by the *PCI Express Base Specification, Revision 1.0*.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Examine the Capability ID fields for each of the device Capabilities.
3. If the Extended Capability ID field of 0003h is found for a capability, the following checks are performed:
 a. The capability version must be 01h.
4. The DWORD at offset 04h is read. (Serial Number register Lower DW). The test logs a warning if the value is zero.
5. The DWORD at offset 08h is read. (Serial Number register Upper DW). The test logs a warning if the value is zero.

6. The Serial Number registers are checked to ensure they are read only.
7. The following register field characteristic tests are performed:

Device Serial Number Enhanced Capability Header

a.	PCI Express Extended Capability ID	RO
b.	Capability Version	RO
c.	Next Capability Offset	RO
d.	Serial Number register (Lower DW)	RO
e.	Serial Number register (Upper DW)	RO

8. The test is repeated with the device under test in D0-Unitialized and D0-Initialized.
9. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- More than one Device Serial Number capability structures are present.
- The capability version for a Device Serial Number Capability does not report 01h.
- Either of the Serial Number registers read zero.
- Either of the Serial Number registers are not read only.
- Any of the register field characteristic tests fail.

3.1.13. Test 1.10 Power Budgeting Capability

This test is run on all device types. The test verifies that if a PCI Express component reports a PCI Express Power Budgeting Capability structure it is implemented as required by the *PCI Express Base Specification, Revision 1.0*.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Examine the Capability ID fields for each of the device Capabilities.
3. If the Extended Capability ID field of 0004h is found for a capability, the following checks are performed:
 a. The capability version must be 01h.
4. Software writes 0h to the Data Select register.
5. Software reads a DWORD from the offset 8 (Power Budgeting Data register).
6. Software performs the following checks on the Power Budgeting Data register:
 a. Software checks that the Power Rail field is one of the defined values (000b, 001b, 010b, or 111b).
 b. Software records the PM State, and Type fields for Power Budgeting Data.
 c. If the Data Scale field is 00b then the Base Power field must not be F3 to FFh.

7. Software repeats steps 4-6 adding one to the last value written to the Data Select register.
8. Software continues until the Power Budgeting Data register reads all zeros.
9. The following register field characteristic tests are performed:

Power Budgeting Enhanced Capability Header

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Data Select Register RW

Data Register

a. Base Power	RO
b. Data Scale	RO
c. PM Sub State	RO
d. PM State	RO
e. Type	RO
f. Power Rail	RO

Power Budget Capability Register

a. System Allocated	HwInit

10. The test is repeated with the indices written to the Data Select register in random order. The returned information must be the same.
11. The test is repeated with an out of bound index used in the first access. The rest of the test must still complete normally.
12. The test is repeated with the device under test in D0-Unitialized and D0-Initialized.
13. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- More than one Power Budgeting Capability structure is present.
- The capability version for the Power Budgeting Capability does not report 01h.
- The form factor for the component under test requires a Power Budgeting Capability and one is not present.
- The device under test reports an illegal Power Rail value for any of the non-zero Power Budgeting Data sets that it reports.
- The component does not report at least a D0 Max and D0 Sustained set of power data for every power rail it uses power from.
- The component under test reports more than one set of data for the same PM State, Type, and Power Rail combination.
- Any of the register field characteristic tests fails.
- The power information is not returned normally when valid indices are used after an invalid index is written to the data select register.

3.1.14. Test 1.11 Command and Status Registers

This test is run on all device types. This test checks updated rules/encoding for Command and Status register fields on PCI Express Devices.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read the word from location 04h in configuration space (Command register).
3. Perform the following checks of fields in the Command register:
 a. I/O Space Enable bits must be R/W
 b. Bus Master Enable must be R/W
 c. Memory Space Enable bits must be R/W
 d. Parity Error Response and SERR# Enable bits must be R/W.
 e. Interrupt Disable must be R/W if the Interrupt Pin register is non-zero. (The Interrupt Pin register is read from offset 3Dh to perform this check.)
4. Read the word from Offset 06h in configuration space (Status register).
 a. Capabilities List – Must be 1.
 b. 66 MHz Capable – Must be zero.
 c. Fast Back-to-Back Transactions Capable – Must be zero.
 d. DEVSEL Timing – Must be zero.
5. The following default value checks are made:

Command Register

a. Bus Master Enable	0
b. Parity Error Response	0
c. SERR# Enable	0
d. Interrupt Disable	0
e. Special Cycle Enable	0
f. Memory Write and Invalidate	0
g. VGA Palette Snoop	0
h. IDSEL Stepping/Wait Cycle Control	0
i. Fast Back-to-Back Transactions Enable	0
j. Reserved	0

Status Register

a. Interrupt Status	0
b. Capabilities List	1
c. 66 MHz Capable	0
d. Fast Back-to-Back Transactions Capable	0
e. Master Data Parity Error	0
f. DEVSEL Timing	0
g. Signaled Target Abort	0

h.	Received Target Abort	0
i.	Received Master Abort	0
j.	Signaled System Error	0
k.	Detected Parity Error	0
l.	Reserved	0

The default value requirement applies to all components except root complexes.

The zero default values on status registers assume that no events that would cause an error indication have occurred in the test environment.

6. The following register field characteristic tests are performed:

Command Register

a.	Bus Master Enable	RW
b.	Special Cycle Enable	RO-Zero
c.	Memory Write and Invalidate	RO-Zero
d.	VGA Palette Snoop	RO-Zero
e.	Parity Error Enable	RW
f.	IDSEL Sleeping/Wait Cycle Control	RO-Zero
g.	SERR Enable	RW
h.	Fast Back-to-Back Transactions Enable	RO-Zero
i.	Interrupt Disable	RW-if Interrupt Pin is non-zero
j.	Special Cycle Enable	RO-Zero
k.	Memory Write and Invalidate	RO-Zero
l.	Reserved	RO-Zero

Status Register

a.	Interrupt Status	RO
b.	Capabilities List	RO
c.	66 MHz Capable	RO-Zero
d.	Fast Back-to-Back Transactions Capable	RO-Zero
e.	Master Data Parity Error	RW1C
f.	DEVSEL Timing	RO-Zero
g.	Signaled Target Abort	RW1C
h.	Received Target Abort	RW1C
i.	Received Master Abort	RW1C
j.	Signaled System Error	RW1C
k.	Detected Parity Error	RW1C
l.	Reserved	RO-Zero

7. The test is repeated with the device under test in D0-Unitialized and D0-Initialized.

8. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The command or status registers cannot be read.
- The interrupt disable bit is not R/W and the Interrupt pin register is non-zero.

- Any of the following fields are not zero: Special Cycle Enable, Memory Write and Invalidate, VGA Palette Snoop, IDSEL Stepping/Wait Cycle Control, Fast Back-to-Back Transactions Enable.
- The Parity Error Enable or SERR Enable bits are not R/W.
- Any of the register field characteristic tests fails.
- Any of the default value checks fail for any component except a root complex.

3.1.15. Test 1.12 Cache Line Size, Master Latency Timer, and Min_Gnt/Max_Lat Registers

This test is run on all device types. This test checks updated rules/encoding for Cache Line size, Master Latency timer, Min_Gnt, and Max_Lat register fields on PCI Express Devices.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read the byte from offset 0Ch in configuration space (Cache Line Size register).
3. Write the inverse of the value read to offset 0Ch.
4. Read the byte from offset 0Ch in configuration space. Verify the value read is the value written in step 3.
5. Read the byte from offset 0Dh (Mater Latency Timer register) in configuration space. The value read must be zero.
6. Read the byte from offset 3Eh (Min_Gnt) in configuration space. The value read must be zero.
7. Read the byte from offset 3Fh (Max_Lat) in configuration space. The value read must be zero.
8. The following register field characteristic tests are performed:

Cache Line Size Register	RW
Master Latency Timer Register	RO-Zero
Min_Gnt	RO-Zero
Max_Lat	RO-Zero

Default Values:

Master Latency Timer Register	0
Min_Gnt	0
Max_Lat	0

9. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The cache line size register is not R/W.
- The master latency timer register does not read zero.
- The Min_Gnt register does not read zero.
- The Max_Lat register does not read zero.
- Any of the register field characteristic tests fails.

3.1.16. Test 1.13 Interrupt Pin and Interrupt Line Registers

This test is run on all device types. This test checks the Interrupt Pin and Interrupt Line registers on PCI Express devices. If legacy interrupt support is indicated the device must also implement a valid MSI capability structure.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read the byte from offset 3Dh in configuration space (Interrupt Pin register). The value must be in the set (0, 1, 2. 3, 4).
3. Read the byte from offset 03Ch (Interrupt Line register) in configuration space.
4. Write the inverse of the byte read in step 3 to location 03Ch.
5. Read the byte from offset 03Ch in configuration space. Verify it is the byte read in step 4.
6. If the Interrupt Pin register had a valid non-zero value – verify that an MSI capability structure is implemented.
7. The following register field characteristic tests are performed

Interrupt Pin	RO
Interrupt Line	RW (if Interrupt Pin is Non-Zero)

8. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The Interrupt Pin register does not read 0, 1, 2, 3, or 4.
- The Interrupt Pin register is non-zero and the Interrupt Line register is not R/W.
- The Interrupt Pin register is non-zero and a valid MSI capability structure is not implemented.
- Any of the register field characteristic tests fails.

3.1.17. Test 1.14 Secondary Latency Timer and Secondary Status Registers

This test is run on devices requiring Type 1 configuration headers. The secondary latency timer and secondary status registers are checked to verify they meet requirements from the PCI Express specification.

Note: This test description applies to all PCI Express components except a PCI Express-to-PCI bridge.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read the byte from offset 1Bh (Secondary Latency Timer). The value must be zero – unless the device type is a PCI Express-to-PCI Bridge.
3. Read the word from offset 1Eh (Secondary Status register).
4. Perform the following checks on the value read in step 3:
 a. 66 MHz Capable – Must be zero.
 b. Fast Back-to-Back Transactions Capable – Must be zero.
 c. DEVSEL Timing – Must be zero.

 Note: These checks do not apply to a PCI Express-to-PCI bridge.
5. The following default value checks are performed (assuming no uncontrolled additional traffic has occurred):

 Secondary Status Register (Offset 1Eh)

 a. Master Data Parity Error 0
 b. Signaled Target Abort 0
 c. Received Target Abort 0
 d. Received Master Abort 0
 e. Received System Error 0
 f. Detected Parity Error 0
 g. Reserved 0

 The default value requirements apply to all components except root complexes.
6. The following register field characteristic tests are performed:

 Secondary Status Register (Offset 1Eh)

 a. 66 MHz Capable RO-Zero
 b. Fast Back-to-Back Transactions Capable RO-Zero
 c. Master Data Parity Error RW1C
 d. DEVSEL Timing RO-Zero
 e. Signaled Target Abort RW1C

f. Received Target Abort RW1C
g. Received Master Abort RW1C
h. Received System Error RW1C
i. Detected Parity Error RW1C
j. Reserved RO-Zero

7. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The secondary latency timer is non-zero for any device except a PCI Express-to-PCI bridge.
- Any of the following values are non-zero for any device except a PCI Express-to-PCI bridge:
 - 66 MHz Capable
 - Fast Back-to-Back Transactions Capable
 - DEVSEL Timing
- Any of the following fields are non-zero immediately following a reset:
 - Signaled Target Abort
 - Received Target Abort
 - Received Master Abort
 - Received System Error
 - Detected Parity Error
- Any of the register field characteristic tests fails.
- The default value requirement applies to all components except root complexes.

3.1.18. Test 1.15 Bridge Control Register

This test is run on devices requiring Type 1 configuration headers. The Bridge Control register is checked to verify it meets requirements from the PCI Express specification.

Note: This test description applies to all PCI Express components except a PCI Express-to-PCI bridge.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read the word from offset 3Eh (Bridge Control register).
3. Perform the following checks on the value read in step 2:
 a. Master Abort Mode – Must be zero.
 b. Fast Back-to-Back Transactions Enable – Must be zero.
 c. Primary Discard Timer – Must be zero.
 d. Secondary Discard Timer – Must be zero.
 e. Discard Timer Status – Must be zero.
 f. Discard Timer SERR Enable – Must be zero.

 Note: These checks do not apply to a PCI Express-to-PCI bridge.

4. Bridge Control register:
 a. Parity Error Response Enable 0
 b. SERR Enable 0
5. The default value requirements apply to all components except root complexes.
6. Note: These checks do not apply to root complex ports. Firmware may initialize these fields to a different value.
7. The following register field characteristic tests are performed:

Bridge Control Register (Offset 3Eh)

a. Parity Error Response Enable	RW
b. SERR Enable	RW
c. ISA Enable	RW
d. VGA Enable (Optional)	RW (RO-Optional)
e. VGA 16-bit Decode (Optional)	RW (RO-Optional)
f. Master Abort Mode	RO-Zero
g. Secondary Bus Reset	RW
h. Fast Back-to-Back Transactions Enable	RO-Zero
i. Primary Discard Timer	RO-Zero
j. Secondary Discard Timer	RO-Zero
k. Discard Timer Status	RO-Zero
l. Discard Timer SERR Enable	RO-Zero

Bridge Control Register Default Value (Offset 3Eh)

a. Parity Error Response Enable	0
b. SERR Enable	0
c. ISA Enable	0
d. VGA Enable (Optional)	0
e. VGA 16-bit Decode (optional)	0
f. Master Abort Mode	0
g. Secondary Bus Reset	0
h. Fast Back-to-Back Transactions Enable	0
i. Primary Discard Timer	0
j. Secondary Discard Timer	0
k. Discard Timer Status	0
l. Discard Timer SERR Enable	0

8. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The Bridge Control register cannot be read.
- Any of the following fields are non-zero for any type 1 device except a PCI Express-to-PCI Bridge:
 - Master Abort Mode
 - Fast Back-to-Back Transactions Enable
 - Primary Discard Timer
 - Secondary Discard Timer
 - Discard Timer Status

- Discard Timer SERR Enable

- Any of the register field characteristic tests fails.
- The default value requirement applies to all components except root complexes.

3.1.19. Test 1.16 PCI Power Management Capability Structure

This test is run on all devices. The test ensures that a valid PCI Power Management Capability structure is present for each PCI Express device.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read the DWORD from offset 00h in the capability (Power Management Capabilities register).
3. The capability ID must be set to 01h for the power management capability.
4. The version must be set to 02h for devices implemented to the *PCI Express Specification, Revision 1.0*.
5. The PME Clock field must be zero.
6. Bits 31, 30, and 27 must be set if the component is a Root Complex port or Switch port.
7. A word is read from offset 04h in the Power Management Capability (Power Management Status and Control).
8. The following checks are performed on the value read in step 7:
 a. Power State must be 00b.
9. Software writes 11b to the PM State field.
10. Software reads a word from offset 04h and verifies the PM State field now reads 11b.
11. The following register field characteristic tests are performed:

Power Management Capabilities Register

a. Capability ID	RO
b. Next Capability Pointer	RO
c. Version	RO
d. PME Clock	RO-Zero
e. Device Specific Initialization	RO
f. AUX Current	RO
g. D1 Support	RO
h. D2 Support	RO
i. PME Support	RO
j. RsvdP	RO-Zero

Power Management Status/Control Register

a. Power State	RW
b. PME Enable	RWS – only if PME is supported.

Note: For a root complex or switch port there is no way to tell whether PME Enable needs to be RWS since the PME support bits must be set for forwarding but do not necessarily indicate that the device can generate PME.

c. PME Status	RW1CS
d. B2/B3 Support	RO-Zero
e. Bus Power/Clock Control Enable	RO-Zero
f. Data	RO
g. No_Soft_Reset	RO
h. RsvdP	RO-Zero

Power Management Capabilities Register Default Values

a. Capability ID	1
b. Version	2 or 3
c. PME Clock	0
d. RsvdP	0

Power Management Status/Control Register Default Values

a. B2/B3 Support	0
b. Bus Power/Clock Control Enable	0
c. RsvdP	0

12. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- A PCI Power management capability is not present.
- More than one power management capability is present.
- The version for the Power Management Capability structure is not 02h.
- The PME Clock field is non-zero.
- A bridge representing a root complex or switch port does not have bits 31, 30, and 27 set in the PME support field.
- The power state field is not zero in the Power Management Status and Control register.
- The device generates PME but bit 8 (PME Enable) is not R/W.
- The power state field cannot be set to D3 and D0.
- The power state field does not read D0 after a reset when the device is in D0 (un-initialized or initialized)
- Any of the register field characteristic tests fails.
- The default value requirement applies to all components except root complexes.

3.1.20. Test 1.17 MSI-X Capability Structure

This test is run on all devices that have an MSI-X capability structure. A device that supports legacy interrupts must have either an MSI or MSI-X capability structure. This test ensures an MSI-X capability implementation meets *PCI Local Bus Specification, Revision 3.0*.

Starting Configuration

This test is run with devices starting in the D0-Uninitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Two bytes are read from Offset 03Ch in configuration space for the device under test. (Interrupt Line register and Interrupt Pin register)
3. If the Interrupt Pin register is non-zero the device must support MSI interrupts.
4. Examine the Capability ID fields for each of the device Capabilities.
5. If the Capability ID of 11h is found the following checks are performed on the MSI-X capability structure
6. Two bytes are read from offset 02h in the MSI-X capability structure. (Message Control register)
7. The MSI-X Enable field must be zero (after reset).
8. The Function Mask field must be zero after reset.
9. The Reserved bit (11) must be zero.
10. The following register field characteristic checks are performed:

CAP ID	RO
Next Cap Pointer	RO
Message Control Register	
a. Table Size	RO
b. Function Mask	RW
c. Reserved	RO-Zero
d. MSI-X Enable	RW
Table Offset/Table BIR Register	
a. Table BIR	RO
b. Table Offset	RO
PBA Offset/PBA BIR	
a. PBA BIR	RO
b. PBA Offset	RO

Message Address

a. Message Address RW

Message Upper Address

a. Message Upper Address RW

Message Data

a. Message Data RW

Vector Control

a. Mask Bit RW

11. The test is repeated with the device is D0-Uninitialized and D0-iniitialized states.
12. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The Interrupt Pin register has a non-zero value and no MSI or MSI-X capability register is present.
- More than one MSI-X capability register is present.
- The MSI Enable field is not zero by default.
- A register field characteristic test fails.

3.1.21. Test 1.18 Base Address Registers

This test is run on all devices. The test ensures that BAR registers on all device types support 64 bit addressing and request at least 128 bytes of memory.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Starting at offset 10h the next 6 (type 0) or 2 (type 1) DWORDs are read. These are the BAR registers.
3. For each BAR register software checks the first bit (Space Indicator). The following checks are performed based on the value in bit zero:
 a. IO Space (1). Bit 1 must be zero.
 b. Memory Space (0).Bit 0 default value must be zero
 c. For all device types except legacy endpoints the Type field must be 10b indicating 64 bit addressing is supported.
 d. For legacy endpoints the Type must be 10b or 00b.

4. The following register field characteristic tests are performed:

 IO Bar Base

 a. Bit Zero — RO
 b. Bit One — RO-Zero

 Memory Bar Base

 a. Bit Zero — RO
 b. Type — RO
 c. Prefetchable — RO

 Memory Bar Base Default Value

 a. Bit Zero — 0

5. The test software writes 0xFFFFFFFF to each BAR register and then reads the response. The size must be 128 bytes or larger. (Bit 7 or higher must be set.)
6. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- Any of the register field characteristic tests fails.
- Any of the default value checks fails.
- A non legacy endpoint has a memory BAR that does not support 64 bit addressing.

3.1.22. Test 1.19 Multi-Function Virtual Channel Capability Test

This test is run on all device types. The test verifies that if a PCI Express component reports a PCI Express Multi-Function Virtual Channel Capability structure it is implemented as required by the *PCI Express Base Specification, Revision 1.1*.

Starting Configuration

This test is run with devices starting in the D0-Uninitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps:

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Examine the Capability ID fields for each of the device Capabilities.
3. If the Capability ID of 0008h is found the following checks are performed on the Multi-Function Virtual Channel Capability Structure.
4. Software reads the DWORD at offset 04h (Port VC Capability Register 1) and performs the following checks:
 a. Checks that the Low Priority Extended VC Count is less than or equal to the Extended VC count.
 b. The Reference Clock field must be zero.

5. Software reads the DWORD from offset 08h (Port VC Capability Register 2) and performs the following checks:
 a. No reserved bits (4-7) in the VC Arbitration Capability field may be set.
 b. The VC Arbitration Capability field must not be zero if the Low Priority Extended VC Count is non-zero.
 c. The VC Arbitration table offset must not be zero if any bit besides bit zero of the VC Arbitration Capability field is set.
6. Software reads the DWORD from offset 0Ch (Port VC Control and Port VC Status) and performs the following checks:
 a. VC Arbitration Table Status reads zero by default.
7. If the default VC Arbitration Select value is an WRR based arbitration method software reads the default values in the VC Arbitration table. These values must all be zero.
8. Software writes each of the supported values indicated by the VC Arbitration Capability field to the VC Arbitration Select field and verifies the value is read back.
9. For each supported WRR arbitration field mechanism software tests loading the table by writing a table of all zeros of the appropriate size to the indicated VC Arbitration table offset. Software then checks that the VC Arbitration Table Status bit has been set. Software then writes the Load VC Arbitration Table field and verifies that the VC Arbitration Table Status bit is cleared by hardware.
10. Step 9 is repeated using all VC entries for the highest supported VC instead of zero.
11. Software verifies that VC Resource Control, Status, and Capability registers are present for each VC supported by the component. (As Indicated by Extended VC Count field).
12. For each Set of VC Control, Status, and Resource Capability registers software performs the following checks:
 a. Function Arbitration Capability: Must not have bit 6 or 7 set (reserved).
 b. TC/VC Map: Must be FFh for the first VC Resource by default.
 c. All other VCs: Must be zero by default.
 d. Software writes each valid TC combination to the field and ensures that the same value can be read back.
 e. Load Function Arbitration Table: Must be zero. (Always returns zero when read.)
 f. Function Arbitration Select: Software writes each supported value from the Function Arbitration Capability field and ensure that the same value is read back.
 g. VC-ID: Software ensures that the value is hard-wired to zero for the first VC Resource.
 h. VC Enable: Software checks that this bit is hardwired to one for the first VS resource.
 i. Function Arbitration Table Status: Must be zero.
14. For each supported WRR based Function Arbitration scheme software writes a table with all values of the minimum Function number. After the first write to the table software verifies that the Function Arbitration Table Status field is set. Software sets the Load Function Arbitration field. Software verifies that the Function Arbitration Table Status bit clear. Step 13 is repeated with a valid arbitration table containing all ports on the switch.

15. The following register field characteristic tests are performed:

Virtual Channel Enhanced Capability Header

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Port VC Capability Register 1

a. Extended VC Count	RO
b. Low Priority Extended VC Count	RO
c. Reference Clock	RO
d. Function Arbitration Table Entry Size	RO

Port VC Capability Register 2

a. VC Arbitration Capability	RO
b. VC Arbitration Table Offset	RO

Port VC Control Register

a. Load VC Arbitration Table	ROZ
b. VC Arbitration Select	RW, but RO if more than one VC in the LPVC group is enabled

Port VC Status Register

a. VC Arbitration Table Status	RO

VC Resource Capability Register

a. Function Arbitration Capability	RO
b. Maximum Time Slots	HwInit
c. Function Arbitration Table Offset	RO

VC Resource Control Register

a. TC/VC Map	RW (except bit zero - RO)
b. Load Function Arbitration Table	ROZ
c. Function Arbitration Select	RW
d. VC_ID	RO for VC0
e. VC_ID	RW for all non VC0
f. VC Enable	RW

VC Resource Status Register

a. Function Arbitration Table Status	RO
b. VC Negotiation Pending	RO

16. The test is repeated with the component in the D0-Uninitialized and D0-Iinitialized states.

17. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- More than one MFVC capability structure is present.
- An MFVC Capability structure is present anywhere except in Function 0 in the Upstream Port of a multi-function device.
- The Low Priority Extended VC Count is greater than the Extended VC count. (Port VC Capability Register 1)

- The reference clock field is not zero. (Port VC Capability Register 1)
- The VC Arbitration Capability field contains a reserved value and the Low Priority Extended VC count field is non-zero.
- The VC Arbitration Table Offset is zero when WRR based VC Arbitration Capabilities are supported.
- VC Arbitration Table Status reads non-zero by default.
- The default VC Arbitration Select value is an WRR based arbitration method and the default VC Arbitration table values are not all zero.
- VC Resource Control, Status, and Capability registers are not present for each VC supported by the component (as indicated by Extended VC Count field).
- A valid Function Arbitration or VC Arbitration table cannot be written.
- Any of the described VC Resource, Control, Status register value checks are not met.
- Any register field characteristic test fails.

3.1.23. Test 1.20 Vendor Specific Capability Test

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps:

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Examine the Capability ID fields for each of the device Capabilities.
3. If the Extended Capability ID field of 000Bh is found for a capability the following checks are performed:
 a. The capability version must be 01h. (Tested with register checking)
 b. The Next Capability Offset must be a value less than the offset of this capability by at least 8 bytes or must be larger than the offset of this capability plus the VSEC Length value.
 c. The value for VSEC Length must be at least 8. (may not be zero)
4. The following register field characteristic tests are performed:

Vendor-Specific Capability Enhanced Capability Header

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Vendor Specific Header

a. VSEC ID	RO
b. VSEC Rev	RO
c. VSEC Length	RO

5. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- More than one Vendor-Specific capability structures are present with the same VSEC ID.
- The capability version for a Vendor-Specific Capability does not report 01h.
- The Next Capability Offset is at least 8 less than the current capability offset or larger than the current capability offset plus VSEC Length
- VSEC Length is 8 or larger.
- Any of the register field characteristic tests fail.

3.1.24. Test 1.21 BIST_Register Test

This test is run on all device types. This test checks updated rules/encoding for BIST registers fields on PCI Express Devices.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read the word from location 0Ch in configuration space
3. Perform the following checks of fields in the BIST register:

 BIST Register Test

 a. BIST Capable RO

4. If BIST Capable is 1b, the following checks are performed:
 a. Write a 1b to Bit 6 (Start BIST) to invoke BIST.
 b. After 2 seconds, read the BIST register and check the following:
 i. Bit 6 (Start BIST) must be zero
 ii. Bits 0-3 (Completion Code) must return zero
 iii. Bits 4,5 (Rsvd) must return zero
5. If BIST Capable is 1b, the following default value checks are performed:
 a. Completion code 0
 b. Rsvd 0
 c. Start BIST 0
6. If BIST Capable is 1b the following register field characteristic tests are performed:

 BIST Register

 a. Completion code RO-Zero
 b. Rsvd RO-Zero
 c. BIST Capable RO
7. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The configuration space registers cannot be read.
- Any of the register field characteristic tests fails.
- Any of the default value checks fail for any component except a root complex.
- If BIST Capable is 1b and 2 seconds after writing 1b to Start BIST, reading the BIST register returns non-zero values for: Completion code, Rsvd, or Start BIST.

3.1.25. Test 1.22 Slot Numbering Capability Test

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Examine the Capability ID fields for each of the device Capabilities.
3. If the Capabilities ID field of 04h is found for a capability, the following checks are performed.
4. Read the byte from offset 02h (Expansion Slot register). If Bit 5 (First in Chassis field) is set, the Chassis Number (offset 03h) must be non zero and unique. (For purposes of this test, a non-zero value is assumed unique.)
5. The following register field characteristic tests are performed:

 Slot Numbering Capability

 a. Slot Numbering Capability ID — RO Default Value: 04h
 b. Pointer to Next ID — RO

 Expansion Slot Register

 a. Expansion Slots Provided — HwInit
 b. First in Chassis — HwInit
 c. Chassis Number register — RW

6. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- For PCI Express-to-PCI Bridge devices:
 - The Expansion Slots Provided field is zero
 - The Chassis Number register is zero and cannot be written with a non-zero value.
 - Any field or register fails the characteristic or default value test.

3.1.26. Test 1.23 PCI Next Capability Pointer Test

This test is run on all device types. This test checks updated rules/encoding for Next Enhanced Capability Pointer registers fields on PCI Express Devices.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read the byte from offset 34h (Capabilities Pointer) in the Configuration Space and perform the following checks:
 a. The lower two bits must be zero (00b).
 b. The value read must be greater than 3Fh and less than FFh.
 c. The value is recorded in a table to check that subsequent Next Cap Pointers do not use the same value (creating a loop of pointers).
3. The value is used to retrieve the Next Cap Pointer of the Capability that the Capabilities pointer is indicating.
4. If the Next Cap Pointer value is not zero the following checks are performed:
 a. The lower two bits must be zero (00b).
 b. The value read must be greater than 3Fh and less than FFh.
 c. The value is recorded in a table to check that subsequent Next Cap Pointers do not use the same value (creating a loop of pointers).
5. Steps three and four are repeated until:
 a. The Next Cap Pointer is zero, or
 b. The Lower two bits are not zero, or
 c. The Value is not greater than 3Fh and less than FFh, or
 d. The Next Cap Pointer Value was used by the Capabilities Pointer or a previous Next Cap Pointer.
6. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The Capability Pointer registers cannot be read or a pointer is invalid.
- Any of the register field characteristic tests fails.

3.1.27. Test 1.24 PCI Express Next Enhanced Capability Pointer Test

This test is run on all device types. This test checks updated rules/encoding for Next Enhanced Capability Pointer registers fields on PCI Express Devices.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read the word from location 100h in configuration space
3. If the value of the line (all 4 bytes) is 0h, there are no Extended Capabilities present. This is acceptable, no further testing is performed. Otherwise, continue with step 4.
4. If the Next Capability Offset field (bits 20-31) value is 0h, there are no further Extended Capabilities present, no further testing is performed. Otherwise, continue with step 5.
5. If the value of the Next Capability Offset is not D-Word aligned (the bottom two bits must be 00b) or the value is not greater than 107h and less than FF9h the test has failed, no further testing is performed. Otherwise proceed to step 6.
6. The value is recorded in a table to check that a subsequent Next Capability Offset does not use the same value. If the value was repeated in a previous Next Capability Offset the test has failed, no further testing is performed. Otherwise proceed to step 7.
7. Read 4 bytes from the offset indicated in the current Next Capability Offset. If the value of the line (all 4 bytes) is 0h, the pointer pointed to a non-valid capability and the test fails, no further testing is performed. Otherwise repeat steps 4 through 7 until no further testing is indicated.
8. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The Enhanced Capability Pointer registers cannot be read.
- Any of the register field characteristic tests fails.
- Any of the default value checks fail for any component except a root complex.
- Any Next Capability Offset:
 - Is not D-Word aligned (the bottom to bits are 00b)
 - Is not zero or greater than 107h and less than FF9h
 - Is a duplicate of a previous Next Capability Offset
 - Points to a D-Word (4 bytes) that is 0h

3.1.28. Test 1.25 Misc Type 0 Config Space Header Register Test

This test is run on all device types. This test checks updated rules/encoding for Configuration registers fields on PCI Express Devices.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read 4 bytes from offset 2Ch (Subsystem ID and Subsystem Vendor ID) and perform the following checks:
 a. If the Device is not a generic system peripheral device (Base class 8: Sub class 0-3):, the Subsystem Vendor ID must a valid value assigned by the PCI-SIG.
 b. For the purposes of the configuration test program, reads of the Subsystem Vendor ID must not return zero or 0xFFFF.
3. Software checks that the Expansion ROM Base Address register does not request more than 16 MB as follows:
 a. Test software writes FFFFFFFFh to the Expansion ROM Base Address register
 b. Test software reads back the value from the Expansion ROM Base Address register. With Bit zero (Expansion ROM Enable) masked, the value read back must be zero or must be equal to or larger than FF000000h.
4. Perform the following checks of fields in the type zero configuration space:

Configuration Space

a. Vendor ID	RO
b. Device ID	RO
c. Revision ID	RO
d. Header Type	RO
e. Cardbus CIS Pointer	RO
f. Subsystem Vendor ID	RO
g. Subsystem ID	RO

Class Code

a. Programming Interface	RO
b. Sub-Class	RO
c. Base Class	RO
d. Header Type	RO

Expansion ROM Base Address Register

a. Expansion ROM Enable	RW
b. Expansion ROM Base Address	RO
c. Reserved	RO-Zero

Configuration Space Default Value

a. Cardbus CIS Pointer 0

Expansion ROM Base Address Register

a. Expansion ROM Enable 0
b. Expansion ROM Base Address 0
c. Reserved 0

5. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The configuration space registers cannot be read.
- Any of the register field characteristic tests fails.
- Any of the default value checks fail for any component except a root complex.

3.1.29. Test 1.26 Misc Type 1 Config Space Header Register Test

This test is run on all device types. This test checks updated rules/encoding for Configuration registers fields on PCI Express Devices.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read 4 bytes from offset 08h (Revision ID and Class Code registers) and perform the following checks:
 a. The Class Code: Base Class field (byte at 0Bh) must not be zero or a reserved value.
 b. A root port, switch port, or PCI Express bridge, must use Base Class 06h and Sub-Class 04h (Sub Class is the byte at 0Ah).
3. Read the byte at 0Eh (Header Type) and check the following:
 a. Mask the Multi function bit and the remaining value (7 least significant bits) must be 0 or 1h.
4. Perform the following checks of fields in the command register:

Configuration Space

a. Vendor ID RO
b. Device ID RO
c. Revision ID RO
d. Header Type RO
e. Cardbus CIS Pointer RO
f. Subsystem Vendor ID RO
g. Subsystem ID RO

Class Code

a. Programming Interface	RO
b. Sub-Class	RO
c. Base Class	RO
d. Header Type	RO

Expansion ROM Base Address Register

a. Expansion ROM Enable	RW
b. Expansion ROM Base Address	RO
c. Reserved	RO-Zero

Configuration Space Default Value

a. Cardbus CIS Pointer	0

Expansion ROM Base Address Register

a. Expansion ROM Enable	0
b. Expansion ROM Base Address	0
c. Reserved	0

6. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The configuration space registers cannot be read.
- Any of the register field characteristic tests fails.
- Any of the default value checks fail for any component except a root complex.

3.1.30. Test 1.27 Multi-Function Test

This test is run on all device types. This test checks to see if devices have mulit-functions and they respond correctly

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read the byte from offset 0Eh (Header Type) in the Configuration Space.
3. If the Multi-Function bit (bit 7) is not set:
 a. Check that the function number is zero.
 b. Check that the device does not respond to configuration requests to other PCI Express or PCI functions with the same Bus and Device number.
4. If the Multi-Function bit is set and the function number is not zero:
 a. Check that function zero is implemented as a PCI Express function and does have the multi-function bit set.

5. If the Multi-Function bit is set and the function number is zero:
 a. Check that at least one other PCI Express function is implemented.
 b. Check all implemented functions for multi function bit set.
 c. Check all implemented functions for the VPD Capability:
 d. If the optional VPD Capability is found, check that either only 1 or all functions implement the VPD Capability.
6. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The Multi-Function bit is not set and the function number is not zero.
- The Multi-Function bit is not set and the device responds to configuration requests to another function. (PCI Express or PCI)
- The Multi-Function bit is set and the device has not implemented function zero as a PCI Express function with the multi-function bit set.
- The Multi-Function bit is set and there is not at least one other PCI Express function implemented.
- If a VPD Capability is present, it is either only in one function or all functions.

3.1.31. Test 1.28 Vital Product Data Capability Test

This test is run on all device types. This test checks to see if devices Support VPD and if supported they are implemented correctly.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read Capability IDs (03h) and determine if VPD is supported.
3. Insure the following fields can be read (and if there are multiple Tags that they can be read): First Tag value, Large Resource Data length, Next Data Offset, Next Tag Value, and End Tag.
4. Perform the following register FIELD CHARACTERISTICS tests:

 Vital Product Data Header

 a. ID RO
 b. Next ID Pointer RO
 c. VPD Address RW
 d. F (flag) RW
 e. VPD Data RW

 Vital Product Data Header Default value

 a. ID 3
5. Bits 16 – 31 of the DWORD at offset 0 in the capability are written at the same time. Bits 16 – 30 are the DWORD aligned address in the VPD storage component of the VPD data (the

bottom two bits, bit 17 and 18, must be zero). Bit 31 is a flag that tells the system to either read from or write to the supplied address. A zero is written to bit 31 along with the address, and software monitors this bit. When it is set to one by hardware, the DWORD at offset 4 is read. It must contain four bytes of data from the VPD storage component. The following checks are performed on the 4 bytes:

a. Byte zero must contain an Identifier String tag matching criteria set out in Appendix I of the *PCI Specification, Rev. 2.3*.
b. Byte one and two must contain the length of the data items.
c. Bytes three to n must contain the data. (Product Name for this first data item.)
d. Software continues to read data four bytes at a time until the specified length has been read.

6. Software reads the next line (TAG) to determine the next Data Type. If the TAG is not an End Tag, the word at bytes 2 and 3 indicate the length of this data item. The length cannot exceed 0x7FFF minus the current offset. If the length does exceed this value, the test fails and is terminated. Otherwise, software continues to read data four bytes at a time until the specified length has been read.
7. Software repeats the process of reading data from the VPD storage component until an end tag is found.
8. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- Configuration Space cannot be read.
- The Tag field cannot be read or is not correct.
- The end Tag does not exist.
- Any of the register field characteristic tests fails.

3.1.32. Test 1.32 PCI-X Capability Structure Test

This test is run on Bridge devices types. This test checks to see if devices Support VPD and if supported they are implemented correctly

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Verify there is a PCI-X device on the secondary side of a bridge.

3. Perform the following register field characteristics tests:

PCI Capability Header

a. PCI-X Capability ID	RO
b. Next Capabilities Pointer	RO

PCI-X Secondary Status Register

a. 64-Bit Device	RO
b. 133 MHz Capable	RO
c. Split Completion Discarded	RW1C
d. Split Completion Overrun	RW1C
e. Split Request Delayed	RO
f. Secondary Bus Mode and Frequency	RO
g. Reserved	RO
h. PCI-X Capabilities List Item Version	RO
i. PCI-X 266 Capable	RO

PCI-X Bridge Status Register

a. Function Number	RO
b. Device Number	RO
c. Bus Number	RO
d. 64-bit Device	RO
e. 133 MHz Capable	RO
f. Split Completion Discarded	RO
g. Unexpected Split Completion	RW1C
h. Split Completion Overrun	RW1C
i. Split Request Delayed	RW1C
j. Reserved	RO
k. Device ID Messaging Capable	RO
l. PCI-X 266 Capable	RO
m. PCI-X 533 Capable	RO

Upstream Split Transaction Control Register

a. Split Transaction Capacity	RO
b. Split Transaction Commitment Limit	RW
c. Split Transaction Capacity	RO
d. Split Transaction Commitment Limit	RW

PCI-X Bridge ECC Control and Status Register

a. Select Secondary ECC registers	RO
b. Error Present in Other ECC Register Bank	RO
c. Additional Correctable ECC Error	RW1C
d. Additional Uncorrectable ECC Error	RW1C
e. ECC Error Phase	RW1C
f. ECC Error Corrected	RO
g. Syndrome	RO
h. Error First (or only) Command	RO
i. Error Second Command	RO
j. Error Upper Attributes	RO
k. ECC Control Update Enable	WT

l. Reserved	RO
m. Disable Split-Bit-Error Correction	RW
n. ECC Mode	RW/RO

PCI-X Bridge ECC First Address

a. PCI-X Bridge ECC First Address	RO
b. PCI-X Bridge ECC Second Address	RO

4. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- Configuration Space cannot be read
- Any of the register field characteristic tests fails.

3.1.33. Test 1.34 Serial Number Test

This test is run on all devices types. This test verifies the Optional Device Serial Number Capability and that it is implemented correctly

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Check to verify that the device Supports Optional Device Serial Number Capability
3. Software performs the following register field characteristics tests:

Device Serial Number Enhanced Capability Header

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Serial Number Register

a. PCI Express Device Serial Number	RO

Device Serial Number Enhanced Capability Header Default Value

a. PCI Express Extended Capability ID	3
b. Capability Version	1
c. Next Capability Offset	000h or greater than 0FFh.

4. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- Registers cannot be read
- Any of the register field characteristic tests fails.

3.1.34. Test 1.39 Multi-Function Device Function Level Reset Test

This test is run on all functions that supports function level reset and are part of a multi-function device. Various fields are changed to non-default values on the function under test. Function level resets are then performed on all functions except the function under test. The registers in the function under test must remain unchanged.

3.1.35. Test 1.42 ACS Extended Capability Structure

This test is run on all device types. The test verifies that if the PCI Express component reports an ACS Extended Capability structure it is implemented as required by the *PCI Express Base Specification, Revision 2.0*.

Starting Configuration

This test is run with devices starting in the D0-Uninitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure in the PCI Express 1.x test considerations document.
2. Examine the Capability ID fields for each of the device Capabilities.
3. If the Capability ID of 000Dh is found the following checks are performed on the ACS Extended capability structure.
4. The device type must be a Root Port, a Downstream Switch Port , an endpoint or an Upstream Switch Port. The type may only be an endpoint or an Upstream Switch Port if it is part of a multi-function device.
5. Two bytes are read from offset 04h in the ACS Extended capability structure. (ACS Capability register).
6. If ACS P2P Request Redirect is set then ACS P2P Completion Redirect must also be set.
7. If ACS P2P Egress Control is 0b then Egress Control Vector Size is undefined.
8. Two bytes are read from offset 06h in the ACS Extended capability structure. (ACS Control register).
9. The following default value rules are checked for the ACS Control register:
 a. ACS Source Validation Enable 0
 b. ACS Transaction Blocking Enable 0
 c. ACS P2P Request Redirect Enable 0
 d. ACS P2P Completion Redirect Enable 0
 e. ACS Upstream Forwarding Enable 0
 f. ACS P2P Egress Control Enable 0
 g. ACS Direct Translated P2P Enable 0

These checks do not apply to a root complex.

10. N bytes are read from offset 08h in the ACS Extended capability structure. (Egress Control Vector). N is equal to ceiling (Egress Control Vector Size / 8) rounded up to a number of bytes that is a multiple of DWORDS.

11. The bit in the Egress Control Vector corresponding to the port number (root port or downstream switch port) or the function number (function in a multi-function device) of the device under test must be RO-zero. The rest of the Egress Control Vector must be RW for the number of bits indicated in the Egress Control Vector Size. Any remaining bits must be RO-Zero (ReservedP). If the device under test is a root port a bit corresponding to an internal port may also be RO-Zero.

12. The following register field characteristic checks are performed:

ACS Extended Capability Header

a.	PCI Express Extended Capability ID	RO
b.	Capability Version	RO
c.	Next Capability Offset	RO

ACS Capability Register

a.	ACS Source Validation (Root ports and Downstream Switch Ports)	RO-One
b.	ACS Source Validation (All other device types)	RO-Zero
c.	ACS Transaction Blocking (Root ports and Downstream Switch Ports)	RO-One
d.	ACS Transaction Blocking (All other device types)	RO-Zero
e.	ACS P2P Request Redirect (Downstream Switch Ports)	RO-One
f.	ACS P2P Request Redirect (Endpoint or Upstream Switch Port not part of a mulit-function device)	RO-Zero
g.	ACS P2P Request Redirect (All other device types)	RO
h.	ACS P2P Completion Redirect	RO
i.	ACS Upstream Forwarding (Downstream Switch Ports)	RO-One
j.	ACS Upstream Forwarding (Root Ports)	RO
k.	ACS Upstream Forwarding (All other device types)	RO-Zero
l.	ACS P2P Egress Control (All device types)	RO
m.	ACS Direct Translated P2P (Downstream Switch Ports)	RO-One
n.	ACS Direct Translated P2P (Root Ports)	RO
o.	ACS Direct Translated P2P (All other device types)	RO-Zero
p.	Egress Control Vector Size	HwInit

ACS Control Register

a.	ACS Source Validation Enable (ACS Source Validation 0b)	RO-Zero
b.	ACS Source Validation Enable (ACS Source Validation 1b)	RW
c.	ACS Transaction Blocking Enable (ACS Transaction Blocking 0b)	RO-Zero
d.	ACS Transaction Blocking Enable (ACS Transaction Blocking 1b)	RW
e.	ACS P2P Request Redirect Enable (ACS P2P Request Redirect 0b)	RO-Zero
f.	ACS P2P Request Redirect Enable (ACS P2P Request Redirect 1b)	RW
g.	ACS P2P Completion Redirect Enable (ACS P2P Completion Redirect 0b)	RO-Zero
h.	ACS P2P Completion Redirect Enable (ACS P2P Completion Redirect 1b)	RW
i.	ACS Upstream Forwarding Enable (ACS Upstream Forwarding 0b)	RO-Zero
j.	ACS Upstream Forwarding Enable (ACS Upstream Forwarding 1b)	RW
k.	ACS P2P Egress Control Enable (ACS P2P Egress Control 0b)	RO-Zero

l. ACS P2P Egress Control Enable (ACS P2P Egress Control 1b) RW
m. ACS Direct Translated P2P Enable (ACS Direct Translated P2P 0b) RO-Zero
n. ACS Direct Translated P2P Enable (ACS Direct Translated P2P 1b) RW
Note: ACS Direct Translated P2P Enable is not tested if ACS Transaction Blocking in the ACS Capability register is one.

13. The test is repeated with the device is D0-Uninitialized and D0-iniitialized states.
14. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

3.2. Chapter 7 Upstream Port Only Tests

This set of tests applies only to upstream ports of switches, bridges, or endpoint devices.

3.2.1. Test 2.1 Configuration Stress Test

This test is run on upstream ports of endpoint devices, switches, and bridges. The test attempts to configure the device under test under a variety of different scenarios.

Starting Configuration

Device under test is completely un-initialized following a reset.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1 with Active State PM disable for both upstream and downstream components.
2. Repeat the configuration sequence for 100 iterations.
3. Set different combinations of upstream and downstream Active State PM States immediately after bus reset.
4. Repeat configuration sequence for 100 iterations under each possible Active State PM upstream/downstream settings.
5. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The device fails to respond to any part of the standard configuration sequence.

3.2.2. Test 2.2 Link Training Stress Test

This test is run on all upstream ports with a known good root complex. The test checks that the device correctly handles link retraining when it is initiated through the Link Control register of the downstream port controlling the device under test.

Starting Configuration

The device is placed into the desired starting state (D0-Initialized or Un-initialized) following the standard initialization sequence in Section 3.1.

Overview of Test Steps

The test software performs the following steps:

1. Test software resets the bus for the device under test.
2. Test software partially configures the device under test – modifying at least one register value from its default value.
3. Test software records the Negotiated Link Width field of the Link Status register for both upstream and downstream components.
4. Test software records the value of the Training Error field of the Link Status register for both upstream and downstream components.
5. Test software sets the Retrain Link field of the upstream components Link Control register.
6. Software monitors the Link Training bit until it is cleared by hardware.
7. Test software records the Negotiated Link Width field of the Link Status register for both upstream and downstream components.
8. Test software records the value of the Training Error field of the Link Status register for both upstream and downstream components.
9. Steps 2-8 are repeated for 100 iterations.
10. The test software repeats the test with the following combinations of Active State PM settings for the upstream and downstream ports:

Upstream Port	**Downstream Port**
Disabled	Disabled
Disabled	L0s Only
Disabled	L0s or L1
L0s Only	Disabled
L0s or L1	Disabled
L0s Only	L0s or L1
L0s or L1	L0s only
L0s only	L0s only
L0s or L1	L0s or L1

11. The test is repeated with the state of the device under test as D0-Initialized and D0-Unitialized.
12. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The reported negotiated link width of the upstream component ever fails to match the negotiated link width of the downstream component.
- A link training error is reported by either the downstream component or the upstream component at any point.
- Link retraining causes the upstream port to reset (restoring default values).

3.2.3. Test 2.3 Device Response To Indicator Control Messages

This test verifies that the device under test continues to be configurable and respond normally when indicator control messages (most likely unsupported) are intermixed with the standard configuration sequence.

Starting Configuration

The device is placed into the desired starting state (D0-Initialized or Un-initialized) following the standard initialization sequence in Section 3.1.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1 with Active State PM disable for both upstream and downstream components.
2. At the end of the configuration sequence test software writes 01 to the Attention Indictor Control register of the downstream port to which the device under test is attached. This causes an ATTENTION_INDICATOR_* message to be sent to the device under test.
3. Test software reads standard configuration registers to ensure that the device under test is still responding normally.
4. The standard configuration sequence described in Section 3.1.2 (D0-Initialized) is run with a random Attention or Power Indicator control message send between every normal configuration access.
5. Step 4 is repeated for 100 iterations.
6. A flood of Attention/Power Indicator control messages (500) are sent to the device under test.
7. Test software ensures the device configuration registers can still be accessed normally.

 Note: If the device under test has Attention and Power Indicators present on the card, test software uses other mechanisms to send unsupported messages to the device under test. (If Possible).
8. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The device under test fails to respond normally to configuration accesses at any time.
- The device under test produces an error in response to an attention or power indicator control message.

3.2.4. Test 2.4 Device Response To Earliest Allowed Configuration Requests After Reset

This test is run on upstream ports of endpoint devices, switches, and bridges. The test attempts to configure the device under test when configuration requests begin as early as allowed after reset.

Starting Configuration

Device under test is completely un-initialized following a reset.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1 with Active State PM disable for both upstream and downstream components. In all cases the first configuration request following reset is sent at the earliest allowed time (100 milliseconds).
2. Repeat the configuration sequence for 100 iterations.
3. Set different combinations of upstream and downstream Active State PM States immediately after bus reset.
4. Repeat configuration sequence for 100 iterations under each possible Active State PM upstream/downstream settings.
5. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The device fails to respond to any part of the standard configuration sequence.

3.2.5. Test 2.5 Device Response to Different Bus and Device Numbers

This test is run on upstream ports of endpoint devices, switches, and bridges. A device is required to view itself as the recipient of any Type 0 configuration request it receives. This test sends requests to the device with different bus and device numbers to test this requirement.

Starting Configuration

Device under test is completely un-initialized following a reset.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1 with Active State PM disable for both upstream and downstream components.
2. At various points in the configuration sequence different device and bus numbers are used in the commands sent to the device under test.
3. Repeat the configuration sequence for 100 iterations.
4. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The device fails to respond to any part of the standard configuration sequence.

3.2.6. Test 2.6 Secondary Bus Reset Effect Test

This test runs only on PCI Express-to-PCI/PCI-X Bridges. This test checks that the Secondary Bus Reset via the Bridge Control register works correctly.

Starting Configuration

This test is run with devices starting in the D0-Unitialized and D0-Initialized states following the standard initialization procedures in Section 3.1. Active State PM states of the upstream and downstream link are disabled for this test.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Verify that a device is present on the secondary side of the bridge.
3. Modify registers on the device on the secondary side of the bridge.
4. A reset of the secondary interface is initiated by software through assertion of the Secondary Bus Reset bit in the Bridge Control register
5. Verify the device on the secondary side of the bridge is reset.
6. The test is run at 5.0 GT/s (for devices that are capable) and 2.5 GT/s.

The test *fails* if:

- The device fails to rest to the default settings

3.2.7. Test 2.7 Link Speed Test

This test is run on upstream ports of endpoint devices, switches, and bridges. The test attempts to configure the device under test with each supported link speed. The system slot used for this test must support 5.0 GT/s signaling.

Starting Configuration

Device under test is completely un-initialized following a reset.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. The target link speed field is set to 2.5 GT/s on the root port of the system slot.
3. Test software sets the retrain link bit in the Link Control register of the system slot.
4. Test software reads the Link Training bit in the Link Status register of the system slot until it reads zero.
5. Test software reads the Current Link Speed in both the system slot and the device under test. The values must indicate 2.5 GT/s.
6. Test software checks the autonomous bandwidth status field in the system slot. It must never be set.

7. Repeat steps 2-6 for 100 iterations.
8. If the Device under test is capable of 5.0 GT/s operation: Steps 2-7 are repeated using the following settings for the target link speed field:

 System Slot 5.0 GT/s

 (Test software verifies that the Target Link Speed on the device under test reads 5 GT/s).

The test *fails* if:

- The device fails to respond to any part of the standard configuration sequence.
- The current link speed does not match the expected speed in any case.

3.2.8. Test 2.8 Supported Link Width Test

This test is run on upstream ports of endpoint devices, switches, and bridges. The test attempts to configure the device under test with each supported link width. The system slot used for this test must support 5.0 GT/s signaling. The system slot used in this test must be a x16 slot that can be configured for x1, x4, x8, or x16 link widths. When the slot is configured for a width smaller than x16 the un-used lanes are not terminated.

Starting Configuration

Device under test is completely un-initialized following a reset.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following procedure described in Section 3.1. The training is done at 2.5 GT/s with the link width of a x16 system slot (with all 16 lanes wired) configured as x1 by placing a x16 to x1 mechanical adaptor in the system slot. All lanes except the configured with for the test are not terminated during the test case.
2. Test software reads the Current Link Speed in both the system slot and the device under test. The values must indicate 2.5 GT/s.
3. Test software reads the Negotiated Link Width field in both the system slot and device under test. The value must indicate x1.
4. Repeat steps 1-3 for 100 iterations.
5. Repeat steps 1-4 with each of the following configured link widths for the system slot (by using mechanical adaptors in the system slot) up to the maximum width supported by the device under test. In each case the Negotiated Link Width in both the system slot and the device under test must match the expected value.
 a. X4
 b. X8
 c. X16
6. If the Device under test is capable of 5.0 GT/s operation, steps 1-6 are repeated training to 5.0 GT/s.

The test *fails* if:

- The device fails to respond to any part of the standard configuration sequence.
- The current link speed does not match the expected speed in any case.
- The negotiated link width does not match the expected width in any case.

3.3. Chapter 7 Downstream Port Only Tests

This set of tests applies only to downstream ports of switches.

3.3.1. Test 3.1 Slot Capabilities, Control, and Status Registers

This test is run on Downstream Ports of PCI Express switches. The test verifies that the PCI Express Slot Capabilities, Control, and Status registers are implemented correctly. The test is only run if the Slot Implemented bit is set in the PCI Express Capabilities register. If the Slot Implemented bit is not set (zero) the Slot Capabilities, Control, and Status registers must be hardwired to zero except for the Presence Detect State field in the Slot Status register which must be hardwired to one.

Starting Configuration

Device under test is completely un-initialized following a reset.

Overview of Test Steps

The test software performs the following steps:

1. Configure the device under test following the procedure described in Section 3.1.
2. Read the four bytes located at offset 14h (Slot Capabilities) in the PCI Express Capability Structure.
3. Read the two bytes located at offset 18h (Slot Control) in the PCI Express Capability Structure.
4. Perform each of the following default value checks on the two bytes read:
 a. Attention Button Pressed Enabled — Zero
 b. Power Fault Detected Enable — Zero
 c. MRL Sensor Changed Enable — Zero
 d. Presence Detect Changed Enable — Zero
 e. Command Completed Interrupt Enable — Zero
 f. Hot Plug Interrupt Enable — Zero
5. Read the two bytes located at offset 1Ah (Slot Status).
6. Perform each of the following checks on the fields in the two bytes read:
 a. Attention Button Pressed — Zero
 b. Power Fault Detected — Zero
 c. MRL Sensor Changed — Zero
 d. Presence Detect Changed — Zero
 e. Command Completed — Zero

The test *fails* if:

- Any of the slot related enable bits are set by default for a non-embedded slot (switch).
- Any of the slot status change/detect bits are set by default for a slot that has just been reset.

3.3.2. Test 3.10 Link Speed Test

This test is run on downstream switch port slots. The test uses a compliant add-in card that supports 5.0 GT/s signaling. The add-in card used for the test has the same physical width as the slot under test.

Starting Configuration

Device under test is completely un-initialized following a reset.

Overview of Test Steps

The test software performs the following steps:

1. Configure the add-in card in the slot under test following the procedure described in Section 3.1 with Active State PM disabled for both upstream and downstream components at 2.5 GT/s.
2. The target link speed field is set to 2.5 GT/s on the system slot.
3. Test software set the retrain link bit in the Link Control register of the system slot.
4. Test software reads the Link Training bit in the Link Status register of the system slot until it reads zero.
5. Test software reads the Current Link Speed in both the system slot and the add-in card. The values must indicate 2.5 GT/s.
6. Test software checks the autonomous bandwidth status field in the system slot. It must never be set.
7. Repeat steps 2-6 for 100 iterations.
8. If the slot under test is capable of 5.0 GT/s operation: Steps 2-7 are repeated using the following settings for the target link speed field:
 System Slot 5.0 GT/s

The test *fails* if:

- The system slot fails to respond to any part of the standard configuration sequence.
- The current link speed does not match the expected speed in any case.

3.3.3. Test 3.11 Supported Link Width Test

This test is run on downstream switch port slots. The test attempts to configure the slot under test with each supported link width. The add-in cards used for this test must support 5.0 GT/s signaling. Add-in cards with widths x1, x4, x8, and x16 (up to the physical width of the slot under test) are used. Alternately, mechanical adaptors may be used to make a single add-in card appear with different widths.

Starting Configuration

Device under test is completely un-initialized following a reset.

Overview of Test Steps

The test software performs the following steps:

1. Configure the x1 add-in card following the procedure described in Section 3.1 with Active State PM disabled for both upstream and downstream components at 2.5 GT/s.
2. Test software reads the Current Link Speed in both the system slot and the add-in card. The values must indicate 2.5 GT/s.
3. Test software reads the Negotiated Link Width field in both the system slot and add-in card. The value must indicate x1.
4. Repeat steps 1-3 for 100 iterations.
5. Repeat steps 1-4 with each of the following add-in card widths up to the maximum width supported by the slot under test. In each case the Negotiated Link Width in both the system slot and the add-in card must match the expected value.
 a. X4
 b. X8
 c. X16
6. If the slot under test is capable of 5.0 GT/s operation: Steps 1-5 are repeated training to 5.0 GT/s.

The test *fails* if:

- The slot fails to respond to any part of the standard configuration sequence.
- The current link speed does not match the expected speed in any case.
- The negotiated link width does not match the expected width in any case.